scalable DAC

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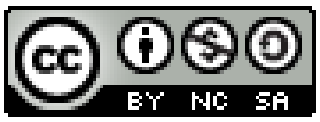

Figure 1: CC-BY-NC-SA

Contents

1 Acknowledgement

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For more information , see https://nlnet.nl/PET or https://ngi.eu.

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2 Principle of DAC

In this section we describe the main operations of a Digital to Analog Converter (DAC).

2.1 DAC Architecture principle

The N-bit DAC takes the N-bit digital signal B_i as input and provides the analog output voltage V_{out} to drive an external load. To meet the driving requirements the DAC uses active elements like op-amps or OTA [1, 2, 3, 4, 5, 6].

DACs are based on a voltage or a current divider. Such a divider can be a passive structure (resistor or capacitor) or an active one (MOS transistor as a current source). Therefore the reference may be attenuated or amplified. The matching and temperature interdependency of the passive and active components will impact the precision of the DAC. Resolution and linearity up to $60dB$ are possible without trimming or calibration [5].

Another important component of the DAC is the switch, made with MOS transistors. Single MOS transistor can be used as a switch between 2 fixed voltages. For switching nodes that experience some swings, complementary transistors (switch based on a NMOS-PMOS pair), or even bootstrap switching structures are preferred [5, 7, 8].

The reference voltage (or current) of the DAC should ensure a high level of accuracy to provide a constant value independent of temperature, input and load variation.

2.2 DAC use and goal of this report

This document investigates simple passive structures, i.e. based on resistor or capacitor dividers, and provides some comparison of DAC features. Note that DAC architectures are often used in ADC architectures such as Successive Approximation Register Analog-to-Digital Converter (SAR ADC) or pipelines ADC.

3 Resistor based architectures

3.1 Integrated resistor

Silicon Integration technologies offer resistive layers which resistance ranges from a few $\Omega/square$ to $k\Omega/square$. When there is choice between different layers, the guiding principle to select the resistive layer is: not too resistive

layer, resulting in non-minimal area to increase accuracy, but resistive enough layer, not to increase too much the area [3].

The absolute value of resistance impacts the power consumption and the speed of the circuit. The relative value of a set of resistances (matching accuracy) impacts gain error and harmonic distortion. The layout is of utmost importance to set the matching.

3.2 R-2R resistor ladder DAC

A string of resistors connected across the high reference and the low reference provides multiple voltages whose digitally controlled selection realizes a basic DAC architecture. It is known as the Kelvin divider [1, 2, 5].

It can be realized using the voltage as signal (called voltage-mode), or the current (called current-mode) with an opamp to adapt the output impedance to its load. Since the number of resistors increases exponentially with the number of bits, the $R-2R$ ladder structure (Fig. 2) has been introduced to solve the problem [9, 10, 7, 11]. It uses a $R-2R$ cell per bit plus a $2R$ terminal, requiring $3n$ resistors instead of 2^n.

The R2-R ladder can be used in *voltage* mode considering the input/output signals as voltages (Fig. 2), or in *current* mode considering that the current is the relevant input/output signal (Fig. 3). In both cases, the supply can be a voltage supply, and an OTA does the voltage/current adaptation for load driving.

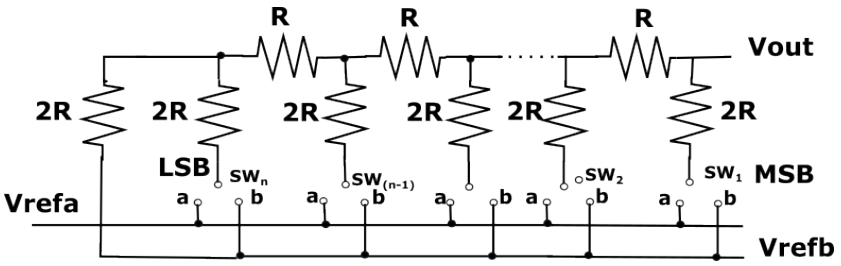

Figure 2: R-2R ladder in *voltage* mode

In the *voltage* mode (Fig. 2), the control bits (the digital word) switch every rung of the ladder either to $Vrefa$ (switch SWi in position a) or to $Vrefb$ (switch SWi in position b). The output of the $R-2R$ ladder, with $Vrefa = Vref$ and $Vrefb = Vss$ is the superposition of terms that are the successive division of $Vref$ by 2. For the digital input $Din = \{b_n, b_{n-1}, ..., b_1\}$ we get the DAC output analog signal ($n-bit$ case):

$$Vout = \frac{Vref}{2}b_n + \frac{Vref}{2}b_{n-1} + ... + \frac{Vref}{2^{n-1}}b_2 + \frac{Vref}{2^n}b_1 \qquad (1)$$

In the *current* mode (Fig. 3), the control bits (the digital word) also switch every rung of the ladder either to $Vrefa$ (switch SWi in position a) or to $Vrefb$ (switch SWi in position b).

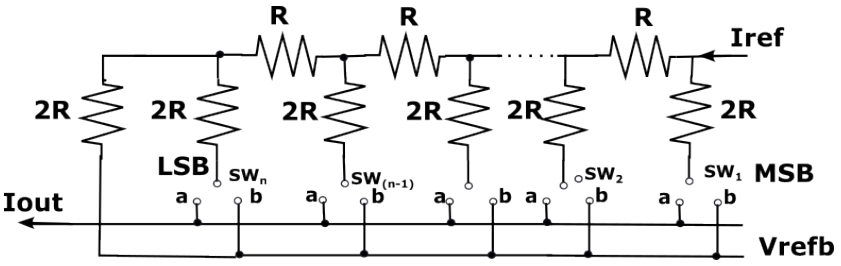

Figure 3: R-2R ladder used in *current* mode

With $Vrefa = Vref$ and $Vrefb = Vss$, the ladder circuit performs a division by 2 of the reference current $Iref$. The superposition of the currents selected by the switches, controlled by the digital input $Din = \{b_n, b_{n-1}, ..., b_1\}$ provides the resulting output current ($n - bit$ case):

$$Iout = \frac{Iref}{2}b_n + \frac{Iref}{2}b_{n-1} + ... + \frac{Iref}{2^{n-1}}b_2 + \frac{Iref}{2^n}b_1 \qquad (2)$$

To adapt the output impedance of the $R - 2R$ ladder, we use a buffer or an OTA with high input impedance, either in non-inverting topology for *voltage* mode (Fig. 4) or in inverting topology for *current* mode (Fig. 6).

3.2.1 Voltage-mode R-2R ladder DAC

Figure 5 shows what is called the *voltage* structure, where the OTA is used in a non-inverting mode (Fig.4). With A the finite gain of the OTA and $Y1 = 1/R1$ and $Y2 = 1/R2$ the voltage gain of the non-inverting structure is in the general case:

$$\frac{Vout}{Vin} = (\frac{A}{1 + A\frac{Y2}{Y1+Y2}}) \qquad (3)$$

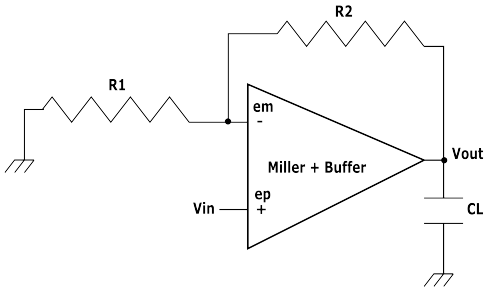

Figure 4: OTA used in a non inverting structure with ideal gain (Eq.4)

which, in the ideal case ($A \to \infty$) gives:

$$\frac{Vout}{Vin} = (1 + \frac{R2}{R1}) \tag{4}$$

The R-2R ladder DAC using the *voltage* structure is presented in Fig.5:

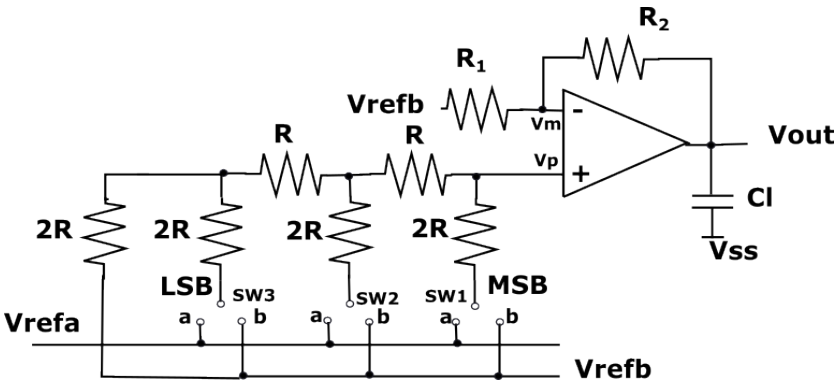

Figure 5: *voltage* mode R-2R ladder DAC using an non-inverting OTA buffer

3.2.2 Current-mode R-2R ladder DAC

Figure 7 shows what is called the *current* mode, where the OTA is used in an inverting mode (Fig.6), with a voltage gain (Eq.5). The $R - 2R$ ladder DAC output current is injected on the *virtual* ground of the OTA (negative input) connected in current/voltage transconductor. The advantage of this architecture is to avoid the problem of common mode stabilization arising in the *voltage* mode for advanced process nodes, with low supply voltage.

This is the classic voltage inverter setup (Fig.6), the DAC resistor being the input resistor $R1$ (Fig. 7) and the feedback resistor $R2$ can be sized to set a possible gain (Eq.6 ideally):

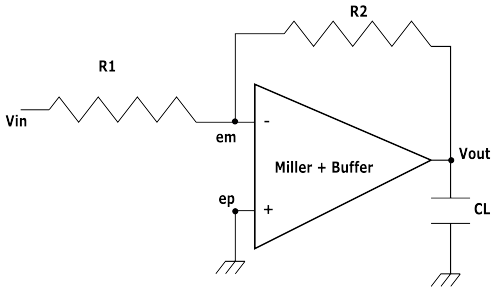

Figure 6: OTA used in an inverting structure with gain (Eq.6)

$$\frac{Vout}{Vin} = \frac{-A\frac{Y1}{Y1+Y2}}{1+(-A\frac{Y1}{Y1+Y2})(-\frac{Y2}{Y1})} \tag{5}$$

which, in the ideal case ($A \to \infty$) gives:

$$\frac{Vout}{Vin} = (-\frac{R2}{R1}) \tag{6}$$

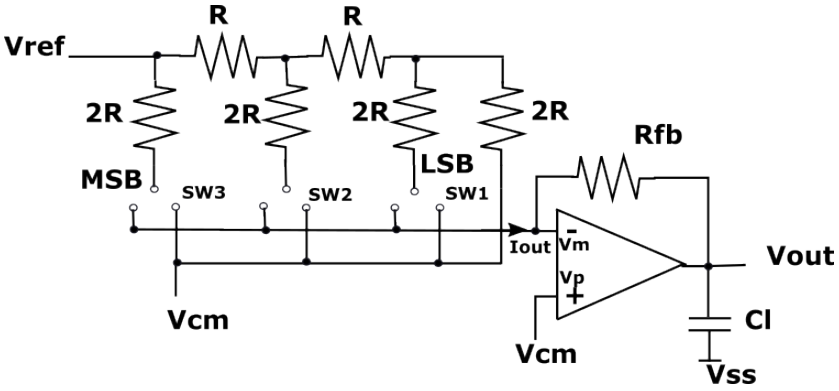

Figure 7: *current* mode R-2R ladder DAC using and inverting OTA structure as buffer

Figs. 8, 9, 10, 11, 12 show some simulation results for a basic 3 bit $R-2R$ DAC, using the ladder architecture presented in Fig. 7, with $Vref = 2.4V$ and several input words Din, using a CMOS 350nm technology ($Vdd = 3.2V$, $Vss = 0.0V$, and $Vcm = 1.6V$).

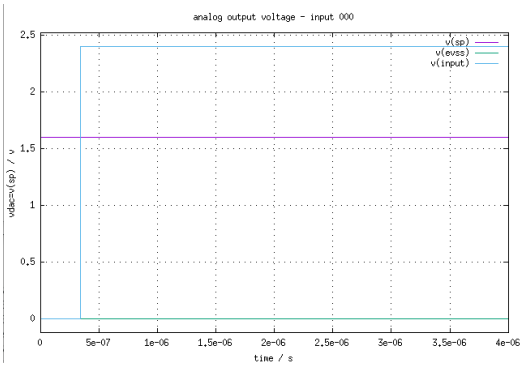

Figure 8: Resistive DAC, Din=000, Fig. 7, $Vout = V(sp)$, $Vref = V(in)$, using a CMOS 350nm technology, $Vdd = 3.2V$, and $Vcm = 1.6V$.

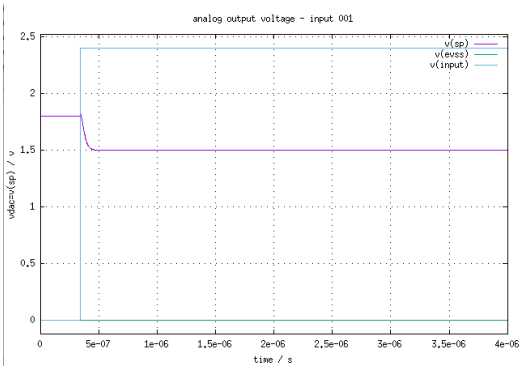

Figure 9: Resistive DAC, Din=001, Fig. 7, $Vout = V(sp)$, $Vref = V(in)$, using a CMOS 350nm technology, $Vdd = 3.2V$, and $Vcm = 1.6V$.

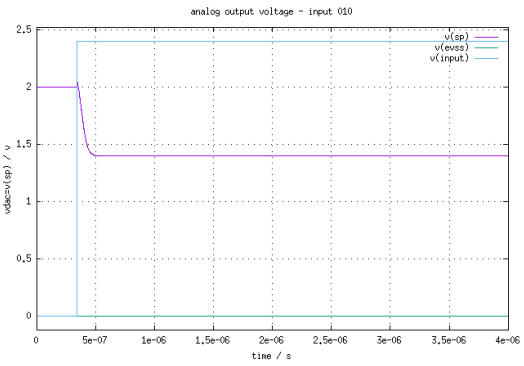

Figure 10: Resistive DAC, Din=010, Fig. 7, $Vout = V(sp)$, $Vref = V(in)$, using a CMOS 350nm technology, $Vdd = 3.2V$, and $Vcm = 1.6V$.

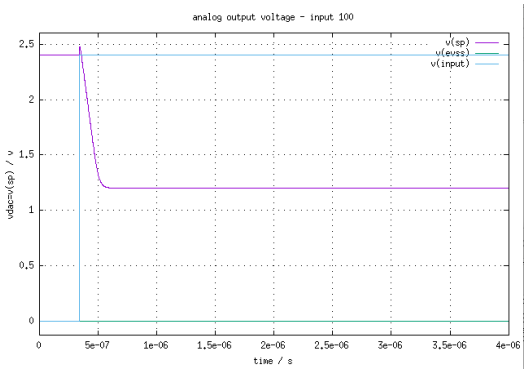

Figure 11: Resistive DAC, Din=100, Fig. 7, $Vout = V(sp)$, $Vref = V(in)$, using a CMOS 350nm technology, $Vdd = 3.2V$, and $Vcm = 1.6V$.

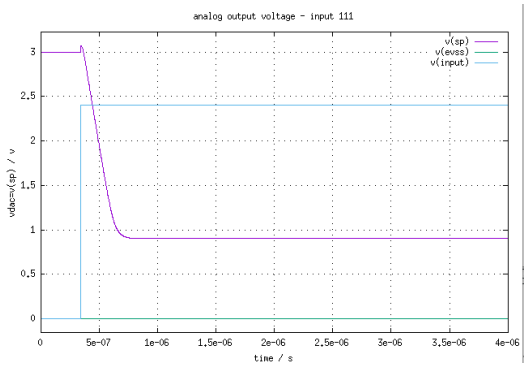

Figure 12: Resistive DAC, Din=111, Fig. 7, $Vout = V(sp)$, $Vref = V(in)$, using a CMOS 350nm technology, $Vdd = 3.2V$, and $Vcm = 1.6V$.

3.2.3 Sizing considerations

Here we provide some guidelines for sizing a $R-2R$ ladder DAC. Some considerations are common either to the *voltage* mode or to the *current* one:

- The advantage of the $R-2R$ ladder DAC is its compact design versus the resistive thermometric design.
- The accuracy of the $R-2R$ DAC is highly dependent on the technology process, and the resistor accuracy. The analog LSB is $Vref/2^n$, directly resulting from $R/2R$ accuracy. The minimal value of resistance is selected to reach the target $R/2R$ accuracy, with acceptable area.
- High accuracy DAC (above 5 bits) require stringent matching between the resistors. This is illustrated by the MSB transition (01111 to 10000) in the 5 bit case. If due to mismatch, the MSB current source (Fig. 7) happens to be less than the sum of the remaining current sources, $Iout$ falls if Din goes from 01111 to 10000. The input-output characteristic of the DAC is not intrinsically monotonous.
- The $R-2R$ resistances have to be high enough versus the reference voltage one.
- The switches resistances have to be low enough versus the $R-2R$ resistance. The switches can be sized based on a binary approach since the current floating through the resistances are binary scaled (see [8]).
- The feedback resistance of the OTA based amplifier $R2$ has to be selected regarding $Vref$, the $R-2R$ resistance R and the OTA based amplifier admissible gain.
- The amplifier can be chosen as a Miller-2-stage OTA, loaded by the feedback resistor, impacting the static gain and the timing response of the DAC. The static gain of the OTA has also a direct impact on the accuracy of the DAC (Eqs. 4, 6). Sizing of the OTA can be performed by Oceane [6].

Moreover, in the *voltage* mode (Fig.5), there are additional considerations to take into account:

- For the choice of $R1$ with a gain $(1+R2/R1)$, $R2$ being chosen, $R1$ can be set depending on $Vref$ and the maximum allowed excursion at the output of the OTA (distortion limit).

- The *output* impedance of the $R-2R$ ladder is constant with Din, which eases the stabilization of the OTA.
- Another drawback of this architecture, is that the reference voltage $Vref$ sees a load that varies with Din.
- When we consider technology migration, another issue is the very high sensitivity to common mode of this architecture, the OTA being used in voltage follower mode (possibly amplified with a resistor in feedback). The two inputs of the OTA differential pair follow the output, and as soon as the supply voltage is lowered, the differential pair will be poorly biased with can degrade the common mode stability.

While, in the *current* mode (Fig.7), there are also other considerations to take into account:

- The voltage of the *virtual* ground Vm and analog ground Vp are equal, the parasitic capacitor of the switched node Vm remains at the same voltage node, whatever Din value is. This has good impact on the switching transient.
- The impedance at the virtual node is dependent on Din, though.
- Glitches may occur during transient.

4 Capacitor based architectures

4.1 Integrated capacitor

Integrated capacitances are made from two conductive parallel plates separated by a thin oxyde and located a few microns or less from the substrate [1, 3, 4]. Integrated technology processes can provide one or several configurations, depending on the layers available in the target process. The unit capacitor may come from one of the main configurations:

- plates one of the top of the other one, the capacitor can be:
  - polysilicon-insulator-polysilicon (PIP), or
  - metal-insulator-metal (MIM)

  in both case, the bottom plate is a usual layer of the process (POLY or METAL), while the top plate is a dedicated layer (special POLY or dedicated METAL-TOP), requiring at least one additional layer compared to the standard digital process.

- plates made by side by side metals, they are metal-oxyde-metal (MOM) capacitors. The characterized devices exist for recent nodes and specific layouts.

Since both PIP and MIM capacitors structures are close to the substrate, the parasitics from the bottom plate to the substate is not negligible. While the bottom plate shields the top plates, the top plate parasitics to the substrate are much smaller than the one of the bottom plate. The parasitic of the plate connected to ground or $Vref$ does not impact the capacitive divider as it receives the required charge through a low impedance node [5]. Therefore it is the bottom plate of the capacitor which is selected to be connected to ground or $Vref$.

To get matched capacitors either with PIP or MIM, dedicated layout are used, such as common centroid ones [12, 13].

The MOM capacitor appeared in more recent nodes, where the distances between metals decrease, giving higher MOM values. To get higher capacitor values, the design of MOM capacitors use finger interdigitated structures. To get matched MOM capacitors, other types of layout arrays are proposed, combining finger interdigitated structures in one metal layer above similar structures in another metal layer [14, 15, 16]. The advantages of MOM capacitors are the following:

- High unit capacitance,
- Low parasitic capacitor with substrate (bottom plate is far from substrate),
- Symmetrical plane structure,
- Excellent RF characteristics,
- Excellent matching characteristics,
- Compatible with metal wire process, no need to add additional process (provided that many available metal layers exist, which is the case in the advanced CMOS manufacturing processes).

4.2 Capacitive DAC

Figure 13 shows a basic capacitive DAC, as commonly used in the capacitive SAR ADCs. The capacitor array, instead of being connected to a comparator is connected to an OTA, using a non-inverting architecture (voltage follower) to adapt the output impedance of the DAC to a loading output. In capacitive

DAC, the capacitor array is such that each capacitor has its bottom plate connected to a reference voltage ($Vref$ or ground).

The circuit operates as follows. The actual digital to analog conversion is preceded by a required reset phase. The goal of the reset phase is to discharge the capacitor array. In the architecture (Fig. 13), the *reset* switch is turned on and the SW_i are on position b so that top and bottom plates are grounded. During the digital to analog conversion phase, the *reset* switch turns off, and the bottom plates are connected to $Vrefa$ or $Vrefb$ (ground) according to the digital word Din. The output voltage for a binary weighted capacitor array, taking into account the parasitic capacitors $C_{p,i}$, with $Vrefa = Vref$ and $Vrefb = 0$, and the digital input $Din = \{b_n, b_{n-1}, ..., b_1\}$ is:

$$Vout = \frac{\sum_1^n b_i C_i}{\sum_0^n C_i + \sum_0^n C_{p,i}} Vref \tag{7}$$

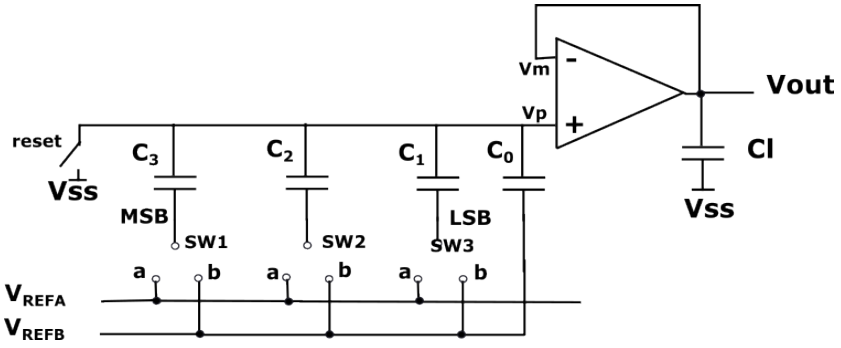

Figure 13: Capacitive DAC with binary weighted capacitors

To get rid of the parasitics $C_{p,i}$, the architecture (Fig.14) has been introduced, using the OTA in the inverting mode. It is more suitable for higher resolutions, reaching 10 bits [2]. The lower plates (Fig.14) are connected to the OTA Vm while the upper plates are connected either to $Vref$ or to the virtual ground Vcm. The DAC operation operates as follows. It also starts with a required reset phase where the capacitive array and the C_T feedback are discharged (reset switch is active and SW_i on position b). Then the actual conversion phase starts, where the upper switches are connected to $Vref$ or Vcm according to the digital word.

As we see, the capacitive DAC is a switched capacitor structure [1]. As it requires a reset phase, it also requires an hold structure to sustain the output.

Figure 15 shows another possible architecture with possible (MDAC), that requires carefully non-overlapping generated clocks, where the $phi1a$

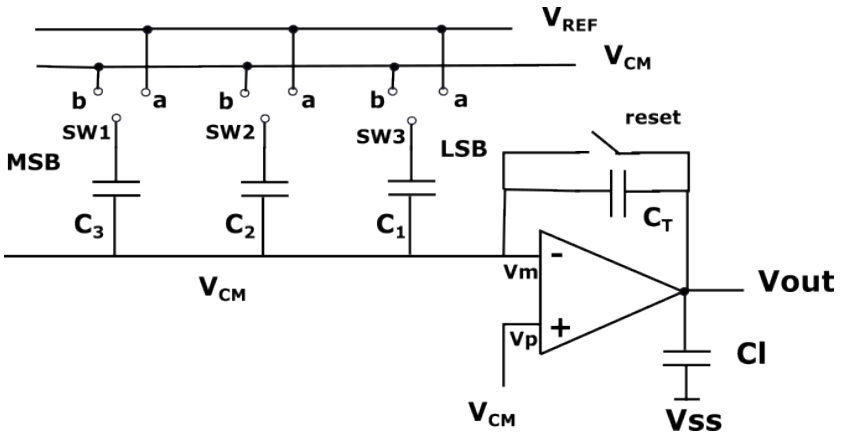

Figure 14: Capacitive DAC

and $phi2a$ signals mean that the clock is slightly advanced with respect to $phi1$ and $phi2$. The digital code should be changed when $phi1$ is active (conversion phase).

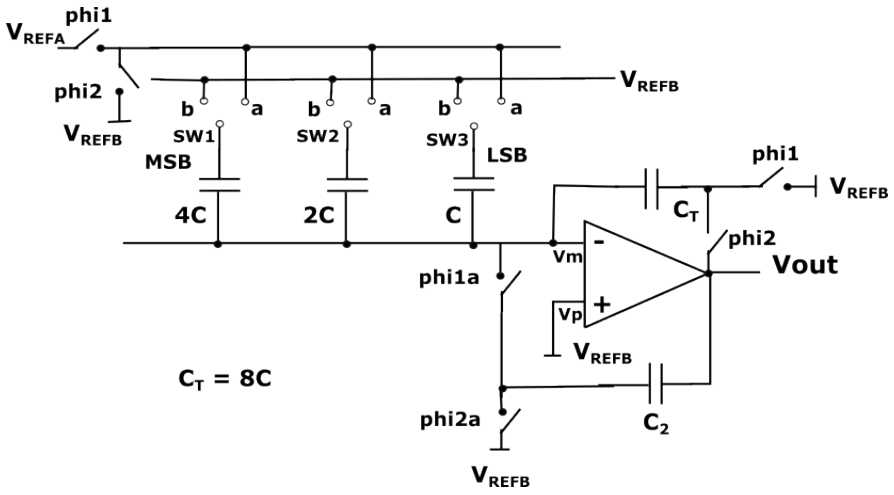

Figure 15: Switched capacitive DAC showing the timing phases $phi1$ and $phi2$ and advanced signals $phi1a$ and $phi2a$ [1]

Figs. 16, 17, 18 show some simulation results for a basic 3 bit capacitive DAC, using only the capacitive array block (capacitors, switches and clocks) presented in Fig. 13, where $PHI1$ activates the reset switch and the digital word and the conversion phase operate when $PHI2$ is active. The control of the SWi switch is $\neg(bi \wedge PHI2)$.

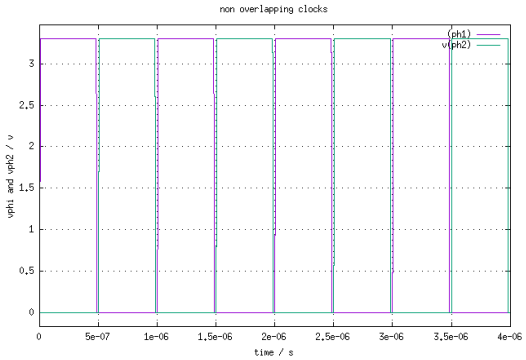

Figure 16: Capacitive DAC: non overlapping clocks PHI1 and PHI2, $Vdd = 3.3V$ and $Vss = 0.0V$

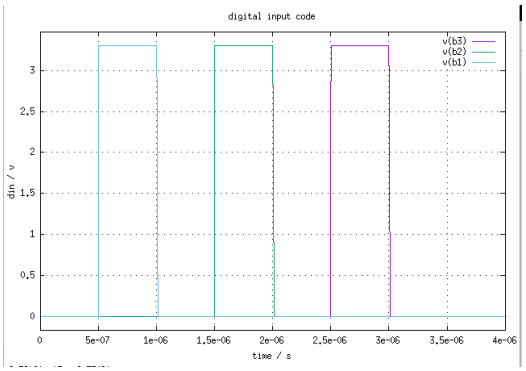

Figure 17: Capacitive DAC: digital input code, $Vdd = 3.3V$ and $Vss = 0.0V$

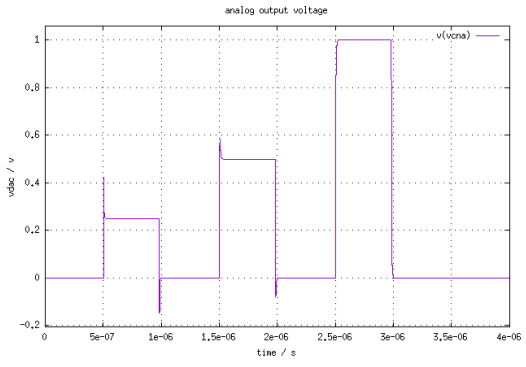

Figure 18: Capacitive DAC: analog output voltage, $Vrefa = Vref = 2.0V$ and $Vrefb = 0.0V$

4.2.1 Sizing considerations

Here we provide some guidelines for sizing the capacitive DAC. The same considerations than in capacitive SAR ADC holds:

- The minimal capacitor value is determined by matching and thermal noise consideration, taking into account the available devices in the target process, the analog LSB $Vref\, C_1/C_T$ results from the matching accuracy of capacitors.
- The switches are sized so that their on-resistance enables to reach the output analog steady state value within the conversion phase [7, 8]. Sizing of the switches can be performed by Oceane [8].
- OTA is sized to have enough DAC gain (allowing virtual ground) and able to load the capacitor within the conversion phase. Sizing of the OTA can be performed by Oceane [6].

5 Comparison

Capacitive dividers and therefore DACs, have pros and cons compared to the resistive ones [2] :

- The power consumption of capacitive DAC is drastically reduced as no DC current flows in the capacitive divider. The energy consumption takes place only during transient: discharging and charging of the capacitors.
- AC and DC behavior of capacitive DACs can be controlled independently.
- The capacitive DAC are very sensitive to parasitics capacitances. Therefore the basic DAC (Fig. 13) can go up to 5 bits without any additional matching strategy. Another architecture, such as (Fig.14), is more appropriate for higher accuracy.
- Resistive DACs are impacted by resistor matching and thermal noise of the resistors, including switches. These non-idealities to be compared to $Vref/2^n$ to estimate the DAC accuracy.
- Capacitive DACs are impacted by the KT/C thermal noise of the switches and the capacitor matching. These non-idealities to be compared to $Vref/2^n$ to estimate the DAC accuracy.

- Capacitive DACs require a reset phase to make sure that the capacitor array is initially discharged. To save the output during reset phase, a hold structure (switched capacitor) is required (Fig.15). Therefore the capacitive DACs require non overlapping clocks.

6 Conclusion

A lot of lectures, PhDs, papers and designs exist on the topic of DAC. Here we focused on simple architectures targetting mature process nodes, and comparison between R-2R ladder topologies versus capacitor ones. Without dedicated trimming techniques, the DACs will provide up to 5 bit accuracy. For higher accuracy, hybrid architectures mixing sub-DACs, or thermometer and R-2R are found [10, 1, 2, 4].

An advantage of the R-2R ladder based DAC is that is requires less switches than the C based DAC. The capacitive DAC is a switched capacitor structure which can take advantage of the MOM capacitor in the recent process nodes. Yet the capacitive DAC requires carefully generated clock waveforms and synchronization with the switching of the digital input code.

The R-2R ladder has more power consumption than the C based DAC.

The choice between a resistive DAC and a capacitiveDAC is highly dependent on the process characteristics and the available devices. As the matching between the passive devices has a big impact on the accuracy of the DAC, the analysis of matching accuracy versus area should be performed to ease the choice. The other major performance is the power consumption of the DAC, which is related to its time performance.

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List of Acronyms

ADC	Analogue-to-digital Converter
DAC	Digital-to-Analogue Converter
CMOS	Complementary Metal Oxide Semi-Conductor
DC	Direct Current (DC analysis or operating point)
EOC	End Of Conversion, to validate the result
SE	Sample Enable signal to activate the input sampling
LSB	Least Significant Bit
MDAC	Multiplying DAC
MSB	Most Significant Bit
SOC	Start Of Conversion, signal to activate the conversion cycle.
V_{DD}	Voltage power supply
V_{REF}	Reference Voltage to perform the conversion steps, it can be equal to the power supply voltage
V_{SS}	Voltage power supply ground