Report on the design of generic VCO IP in CMOS technology

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Avant propos

1 Description of the VCO architecture

The VCO is a ring oscillator composed from a looped chain of individual inverting delay cells. The delay cells are CMOS invertors where the currents of the transistors are controlled by two current limiters MPC and MNC. The control of the MNC current source is achieved directly by the input control volage V_{ctrl}, the transistors MP1 and MN1 generates a control voltage for the P transistor (MP1 and MPC, MN1 and MNC form current mirrors with ratio 1 :1).

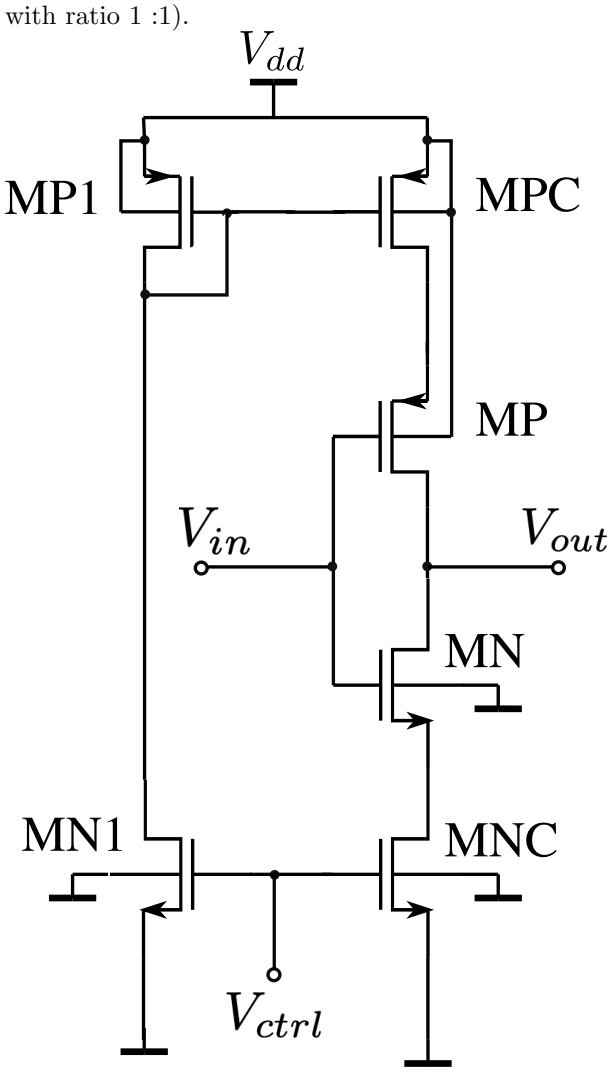

FIGURE 1 – Schematic of a delay cell.

The delay of a CMOS invertor can be estimated, considering that that the output (load) capacitor charges from 0 or discharges from Vdd to Vth=Vdd/2 through the transistors PMOS or NMOS which can be seen as controlled current

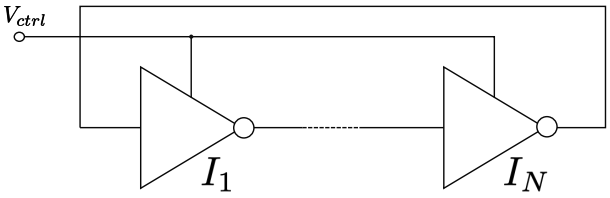

FIGURE 2 – Architecture of the VCO.

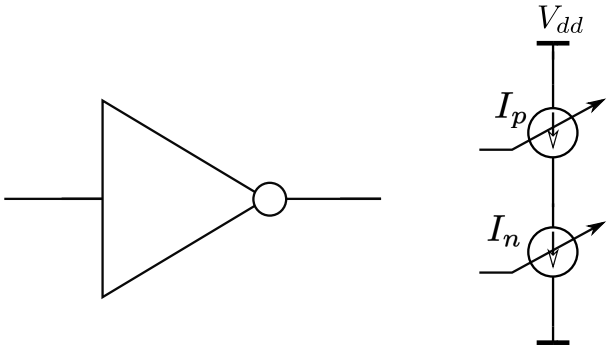

FIGURE 3 – Invertor switching model.

sources (fig. 3), see J. Rabaey, Digital Integrated Circuits, sec. 3.3.

These transistors may be considered as being in saturation all the time till the output capacitor voltage reaches Vdd/2. During this time the current source (the transistor MP or MN) generate a current I_{ch}. Hence, as the input changes from 0 to 1 (for example), the output capacitor C_L needs some time to discharge from Vdd to Vdd/2 through the nMOS transistor (fig. 4). This he delay is given by

$$\tau_d = \frac{Q}{I_{ch}} = \frac{C_L Vdd/2}{I_{ch}} \qquad (1)$$

Here Q is the total charge variation on the capacitor while the output voltage goes from 0 or 1 to $Vdd/2$.

If cell is well balanced, the charge and discharge currents are equal and the above defined quantity τ_d may be considered as the delay of the cell.

Hence, the frequency of a ring oscillator composed out N such cells (N is odd) is given by

$$f = \frac{1}{2N\tau_d} = \frac{I_{ch}}{NC_L Vdd} \qquad (2)$$

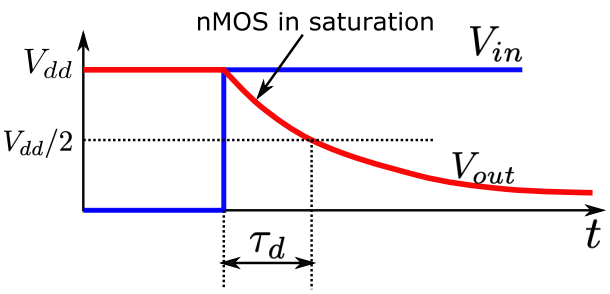

FIGURE 4 – Invertor switching diagram (from 1 to 0).

The load capacitor C_L is composed of the output capacitors of the cell and of the input capacitors of the subsequent cell in the chain.

The cell capacitors can be obtained from the operating point analysis performed with the following biasing : $Vgs = Vds = \pm Vdd/2$ according to the type of the transistor.

The simulator provide the value of the total capacitors connected to the drain and gate nodes, *cgg* and *cdd*. The total load cacitance is the sum of the drain and gate capacitors of PMOS and NMOS transistors, $C_l = cggn + cddn + cggp + cddp$.

The current I_{ch} is calculated for one of the transistors with $Vgs = Vds = \pm Vdd$.

This calculation allows one to obtain the maximum oscillation frequency, when the control voltage is maximum (Vdd) and when the current limiting transistors are much larger than the cell transistors. Typically, when the ratio between the widths of the core transistors MN and MP W_n, W_p and the current limiting transistors MNC and Mpc W_{nc}, W_{pc} defined as $K = W_c/W$ is equal to 3, the presence of the current limiting transistors has negligitble impact on the maximum osillating frequency.

As the ratio K is reduced (e.g., to 1), even when V_{ctrl} has a maximum value (Vdd) , the maximum oscillating frequency is less than one predicted by the formulae (1), and needs to be determined by simulation.

The ratio K should not be too big, sine if MPC and MPN are large, the input capacitance of the *ctrl* input is larger and the control will need more power. We advise the optimal ratio K. Its value should only be increased if a higher oscillation frequency is required, and the maximum value shold be K.

2 Sizing algorithm

Here we describe the sizing algorithm. The example of its application will be given for the technology AMS C35 (350 nm), with the target maximum frequncy of the VCO 300 MHz.

1. The first step consists in sizing a balanced CMOS cell with $Vth = Vdd/2$. For that :
   (a) We fix W_n to the minimum value of the technology, W_{nmin}
   (b) We calculate the current I_n of the nMOS transistor for $Vgs = Vds = Vdd/2$
   (c) We calculate the width of the pMOS transistor W_p for $Vgs = Vds = -Vdd/2$ so to obtain the current I_n determined in the previous step.

   Result of the test case : the ratio is 3.2.

   Only the ratio between the widths W_p and W_n is relevant. The frequency of the ring oscillator does not change is all widths are multiplied by a factor. This is true in "old" technologies, where transistor parasitic capacitors dominate comparing to the wire capacitors. It is less true for deep submicronic technologies, where the layout design may have a strong impact on the oscillaton frequency especially when the transistor sizes are close to the minimum.

2. Before performing the sizing, we provide the characterisation of a 5 stage oscillator for a given technology with the following parameters :
   (a) L=Lmin, K=3, Vctrl=0...Vdd

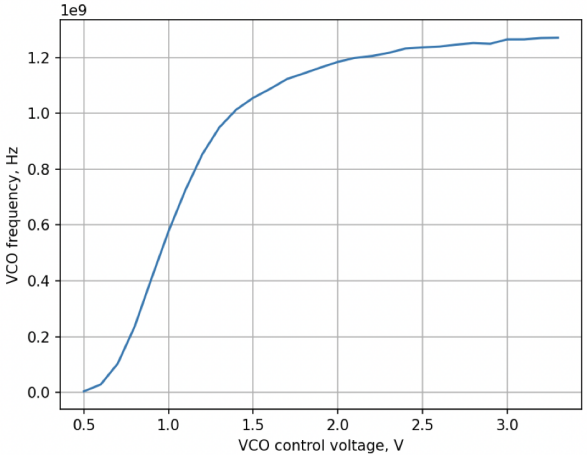

FIGURE 5 – Oscillating frequency vs V_{ctrl} frequency : minimum L, K=3, application to the selected test case.

   (b) For $V_{ctrl} = Vdd$ the corresponding oscillation frequency is the maximum that can be achieved.

   K=3, Vctrl=Vdd, L=Lmin...1um

FIGURE 6 – Oscillating frequency vs L : $V_{ctrl} = Vdd$, K=3, application to the selected test case.

   This gives as the idea about how the maximum oscillation frequency changes with L.

3. After having a look on the two characteristics mentioned above, the user proposes the maximum oscillation frequency, f_{max}.

4. We measure the frequency f_{max1} corresponding to $V_{ctrl} = 0.8Vdd$, $L = Lmin$ and $K = 1$.
5. If $f_{max} < f_{max1}$: the sizing is feasible, go to the step 5.
6. If $f_{max} > f_{max1}$: we try to increase K setting $K = 3$. For $V_{ctrl} = 0.8Vdd$, $L = Lmin$ and $K = 3$ we obtain a new frequency, f_{max2}.
7. If $f_{max} > f_{max2}$: the sizing is impossible and the user should reduce the requested frequency. The procedure stops.
8. Now we look for L (by increasing L) which gives the target f_{max} for $V_{ctrl} = 0.8Vdd$ and $K = 1$. Since the function "Frequency versus L" is strictly monotonic (decreasing), the finding algorithm is straightforward (e.g., the dichotomy), see the code for a practical implementation.
9. We display the output of a working oscillator for the calculated L ad for the input voltages $V_{ctrl} = 0.8Vdd$ ad $V_{ctrl} = 0.3Vdd$.
10. We display the voltage-frequency characteristics of the obtained VCO.

FIGURE 7 – Final voltage-frequency characteristic of the VCO for the test case.

3 Determination of the oscillating frequency

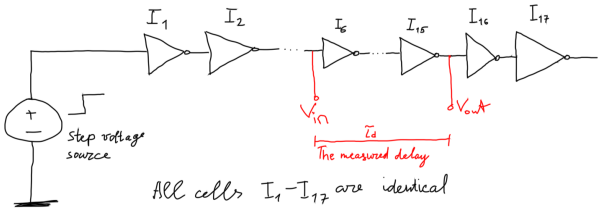

FIGURE 8 – Schematic allowing a measurement by simulation of a cell delay in the conditions identical to those of a ring oscillator.

Direct simulation of an oscillator for determination of the oscillation frequency is not convenient, since the simulation of an oscillator is generally an hazardous job (start-up problems, precision, adjustment of the simulation time to the frequency...). For this reason, the oscillation frequency is calculated from the delay of the cell, which is obtained by simulation of a chain of cells. This is much more robust and fast, because the circuit is open loop and the timing is easier to master. In order to get a realistic estimation of the delay, we simulate a chain of 17 identical cell, and we measure the delay between the input of the cell 6 and the output of the cell 15, see fig. 8. This yields 10 times the delay we want to determine. The fact of using 10 cells improve the precision of the measurement.

This is implemented in the netlist CMOS_delay_cell.scs.

The script calculating the delay of a cell with given parameters (transistor sizes, supply voltage, control voltage, etc.) is given in file CMOS_delay_cell.py.

4 Appendix : results of the application of this sizing procedure to different technology and use cases

4.1 AMS C35 350 nm CMOS

Ratio between the width of the pMOS and nMOS transistors in a threshold balanced CMOS cell is 3.18.

Technology limit plots :

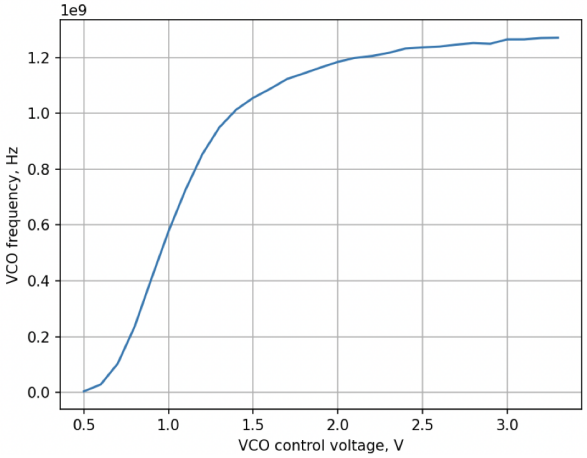

FIGURE 9 – Frequency versus control voltage for the minimum L and for the maximum K=3. Technology AMS C35 350 nm.

4.1.1 Case1 : $F_{max} = 1GHz$

Sizing results : L=420 nm, K=1.

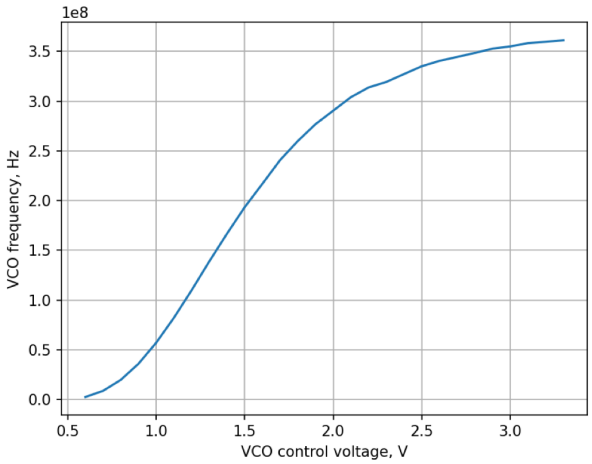

FIGURE 10 – Frequency versus length for the maximum control voltage and for the maximum K=3. Technology AMS C35 350 nm.

FIGURE 12 – Frequency versus control voltage for the specification $F_{max} = 300MHz$. Technology AMS C35 350 nm.

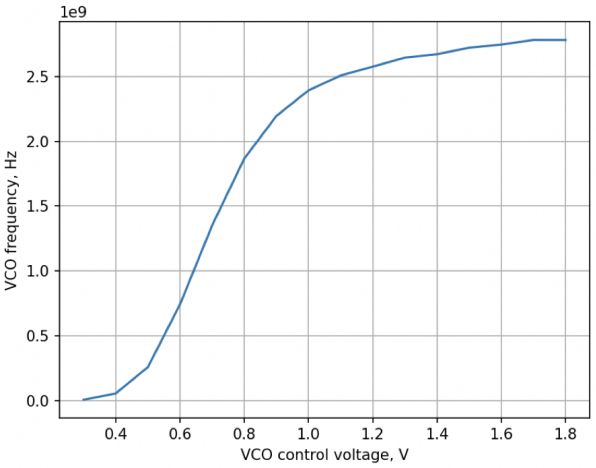

FIGURE 11 – Frequency versus control voltage for the specification $F_{max} = 1GHz$. Technology AMS C35 350 nm.

FIGURE 13 – Frequency versus control voltage for the minimum L and for the maximum K=3. Technology TSMC 180 nm.

4.1.2 Case1 : $F_{max} = 300MHz$

Sizing result : L=678 nm, K= 1.

4.2 TSMC 180 nm CMOS

Ratio between the width of the pMOS and nMOS transistors in a threshold balanced CMOS cell is 3.18.

Technology limit plots :

4.2.1 Case1 : $F_{max} = 1GHz$

Sizing results : L=260 nm, K=1.

4.2.2 Case2 : $F_{max} = 300MHz$

Sizing result : L=547 nm, K= 1.

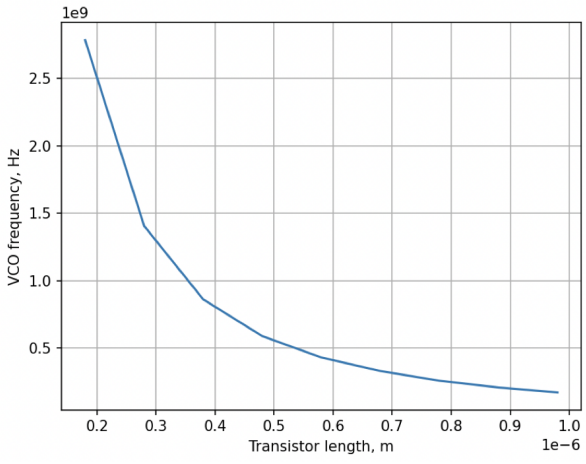

FIGURE 14 – Frequency versus length for the maximum control voltage and for the maximum K=3. Technology TSMC 180 nm.

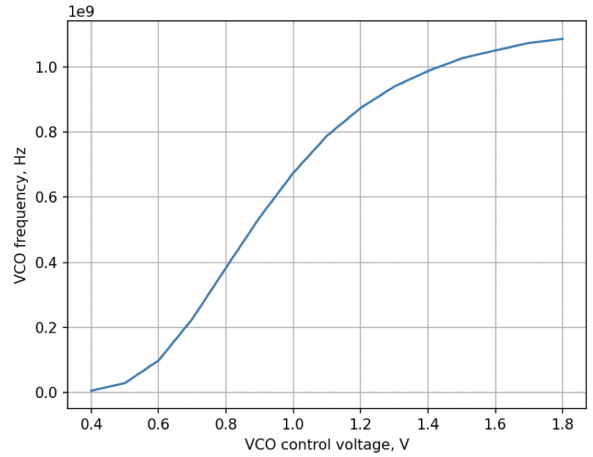

FIGURE 15 – Frequency versus control voltage for the specification $F_{max} = 1GHz$. Technology TSMC 180 nm.

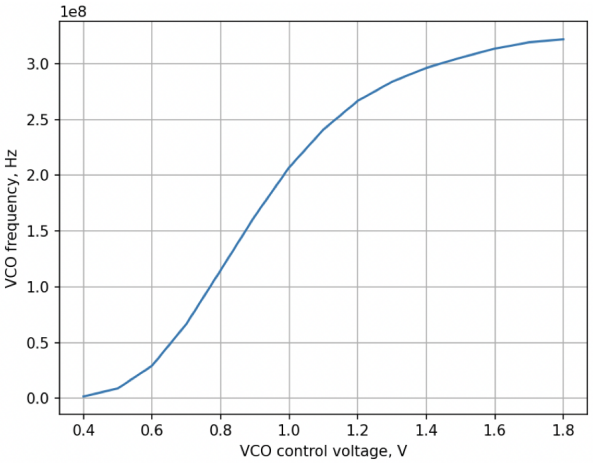

FIGURE 16 – Frequency versus control voltage for the specification $F_{max} = 300MHz$. Technology TSMC 180 nm.

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