scalable SAR ADC

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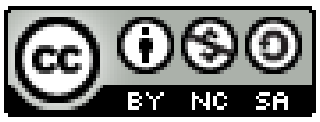

Figure 1: CC-BY-NC-SA

Contents

1 Acknowledgement

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For more information , see https://nlnet.nl/PET or https://ngi.eu.

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2 Principle of SAR ADC

In this section we describe the main operations of the Successive Approximation Register Analog to Digital Converter (SAR ADC).

2.1 SAR ADC Architecture principle

The N-bit SAR ADC takes the analogue signal V_e as input and provides the N-bit digital output B_i. It is a feedback system [1], with a Digital to Analogue Converter (DAC) in the feedback loop. The comparator drives a digital control block, that computes the N-bit input of the DAC SB_i and stores the N-bit output result B_i. Assuming that the gain of the loop is infinite and that the comparator has no offset, the DAC performances set the ADC ones.

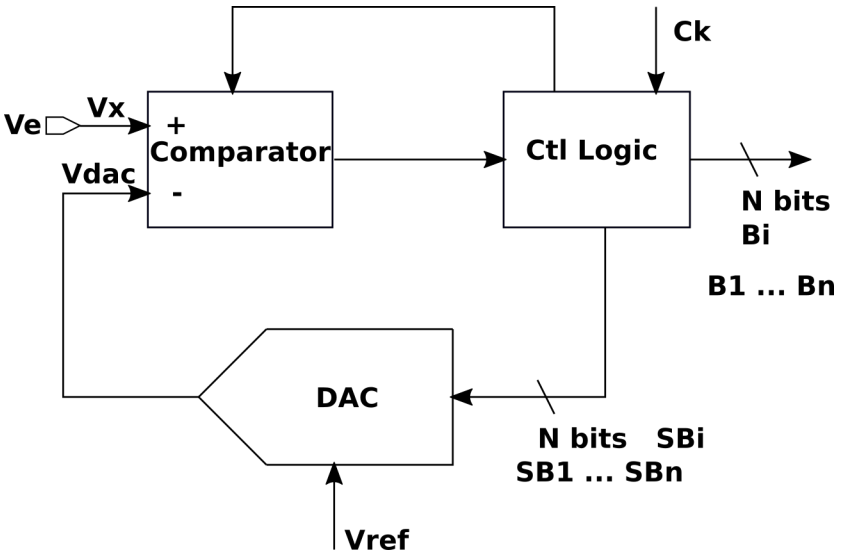

Figure 2: SAR blocks: DAC, comparator and control logic (SAR registers)

2.2 Analogue-to-Digital Conversion algorithm

The algorithm used to compute the digital output is based on a binary search (Fig. 3). At each clock cycle (Ck), the test interval is divided by 2, till reaching the Least Significant Bit (LSB) interval. In the first clock cycle, the Most Significant Bit (MSB) is set to 1, while all the other bits are set to 0, therefore the DAC output is $V_{dac} = V_{REF}/2$, where the reference voltage

V_{REF} is often set to V_{DD}. This voltage V_{dac} is compared to V_x. If V_x is greater than V_{dac}, the MSB remains set to 1, otherwise, it is set to 0. All the bits are computed, one after the other, at each clock cycle (Fig. 3), till reaching the LSB, where the End Of Conversion (EOC) signal is raised.

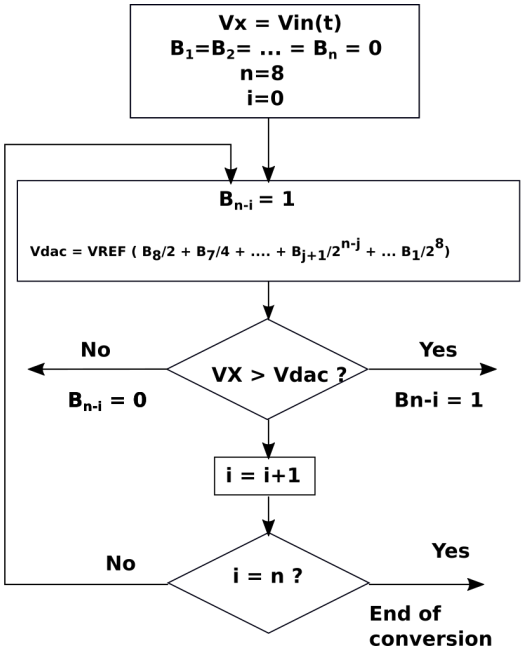

Figure 3: SAR conversion: binary search algorithm

For example, $V_e = V_x = 2,6V$ with $V_{REF} = 4V$ and $N = 8$, runs 9 clock cycles as presented in Table 1, where we want to highlight that **before starting the conversion** : $B_1 = B_2 = B_3 = B_4 = B_5 = B_6 = B_7 = B_8 = 0$

2.3 Sampling consideration at ADC input

Here we want to highlight the role of the sample and hold block to freeze the input signal during the conversion cycle. Let $Ve(t) = A\ sin(\omega t)$ being the input signal, its maximal variation speed is:

$$\frac{dVe(t)}{dt}_{t=0} = A\omega = 2\pi FA, \tag{1}$$

with F_h being the clock frequency and T_h being the clock period, the maximum frequency Fu_{max} which can be used for the input signal frequency F, without Sample and Hold operation, assumes that the input signal am-

nc	B_i set at 1	V_{dac} (V)	V_x and V_{dac}	B_i result
0	B_8	2	$V_x > V_{dac}$	$B_8 = 1$
1	B_7	3	$V_x < V_{dac}$	$B_7 = 0$
2	B_6	2.5	$V_x > V_{dac}$	$B_6 = 1$
3	B_5	2.75	$V_x < V_{dac}$	$B_5 = 0$
4	B_4	2.625	$V_x < V_{dac}$	$B_4 = 0$
5	B_3	2.5625	$V_x > V_{dac}$	$B_3 = 1$
6	B_2	2.59325	$V_x > V_{dac}$	$B_2 = 1$
7	B_1	2.609375	$V_x < V_{dac}$	$B_1 = 0$
8 = N		EOC	$V \sim 2.609375$	

Table 1: Example of conversion, using 8 bits

plitude variation in one full conversion cycle ($N.T_h$) is less than one LSB ($A = 2^N LSB$), so:

$$Fu_{max} = \frac{LSB}{N\ T_h}\ \frac{1}{2\pi A} = \frac{F_h}{\pi N 2^{N+1}}. \tag{2}$$

For example, a 8 bits ADC with F_h at 1MHz and without sample and hold operation, sets a maximum signal frequency of 70Hz.

The sample and hold function can be realised by an explicit sample and hold block (Fig. 4), or implicitly by a convenient configuration of a switch between the input signal and the capacitive DAC (Fig. 6).

Considering the input sampling phase, the input voltage charges a sampling capacitor C_{tot} through a switch with on resistance R_{on}. At the sampling time, the switch turns off, thus holding the value of the input voltage across the capacitor. The sampling operates correctly if the time constant $\tau = R_{on}C_{tot}$ is negligible with respect to the sampling time. Moreover, the bandwidth of the input signal must be much smaller than $1/\tau$ [2].

2.4 ADC operation principle

The netlist in Fig. 4 represents a basic design of the ADC operation principle described in Fig. 2. The DAC is a switched capacitor array, where the capacitors are binary weighted. The sum of all capacitors is $2^N C$. The sample and hold can be a capacitor loaded by a CMOS switch, possibly bootstrapped, to limit the non-linearities coming from the floating nodes of this switch.

To properly initialise the conversion sequence, all DAC capacitors are discharged, while the input signal V_e is sampled (the switch S_0 is on, activated by the Sampling Enable SE control signal, to connect the bottom plate of the capacitors to ground, while the input signal V_e is sampled, with the sampling

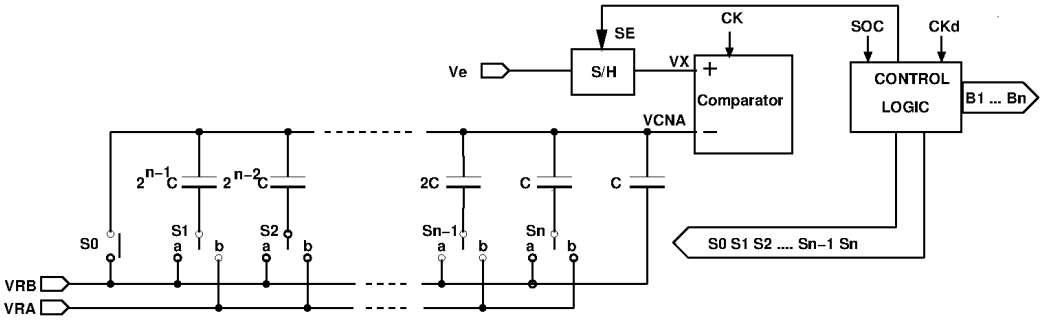

Figure 4: schematic of the non differential SAR ADC with explicit sample & hold block. Usually $V_{RA} = V_{REF} = V_{DD}$, and $V_{RB} = V_{SS} = 0$

switch activated also by SE). Then, during conversion, according to the comparator result at each clock cycle, for each capacitor $2^{(N-i)}C$:

- the switch S_i connects the bottom plate of the capacitor $C_{(N+1-i)} = 2^{(N-i)}C$ to V_{RA} through node **b** (when $B_{(N+1-i)} = 1$), or
- the switch i connects the bottom plate of the capacitor $C_{(N+1-i)}$ to V_{RB} through node **a** (when $B_{(N+1-i)} = 0$).

C_x being the parasitic capacitor on the DAC output node V_{CNA}, the ADC behaves like a capacitive divider (Fig. 5) such that:

$$V_{CNA} = \frac{V_{RA}.C_A + V_{RB}.C_B}{C_A + C_B + C_x} \tag{3}$$

$$C_A = \sum_{i=1}^{N} B_{N+1-i} 2^{N-i} C \tag{4}$$

$$C_B = \sum_{i=1}^{N} \overline{B}_{N+1-i} 2^{N-i} C = 2^N C - C_A. \tag{5}$$

Assuming that we neglect C_x,

$$V_{CNA} = \sum_{i=1}^{N} B_{N+1-i} \frac{V_{RA}}{2^i} + \sum_{i=1}^{N} \overline{B}_{N+1-i} \frac{V_{RB}}{2^i}. \tag{6}$$

After the sample and hold step, V_{CNA} is compared to the input signal V_e. After N elementary comparisons, V_{CNA} converges to the digital signal closest to V_e. Typically, $V_{RA} = V_{REF}$ and $V_{RB} = V_{SS} = 0$, so we get:

$$V_{CNA} = \sum_{i=1}^{N} B_{N+1-i} \frac{V_{RA}}{2^i}. \tag{7}$$

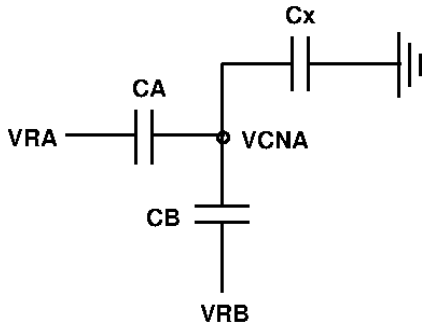

Figure 5: DAC equivalent circuit: a capacitive divider

2.5 Various architectures of the SAR ADC

DAC: The DAC is the main component of the SAR ADC. The advantage of the capacitive DAC is that it has no DC power consumption, the capacitors can be integrated in CMOS processes with a good accuracy. The binary weighted structure allows up to 10 bits accuracy, for 10 MHz and 10 fJ/conversion step. The drawback is the large area required by the binary weighted values of the capacitors. The capacitive DAC is a capacitive array controlled by a set of switches, to set the voltage biasing the capacitor plates, and to activate the sharing or redistribution of charges during the conversion steps.

There are other types of DACs : resistive, switched currents, that we will not discuss here.

Sample and hold: Depending on the DAC, and on how the input signal is sampled, this block may be implicitly provided by the DAC:

- If the input signal is a direct input of the comparator, it requires an explicit S/H block (Fig. 4).
- If the input signal is sampled on a DAC capacitor plate (Fig. 6), adding an explicit S/H block may be avoided.

Comparator: The comparator is a synchronous one, clocked at Ck or H (Fig. 4 and 6), with an RS flip-flop at the output to freeze the comparison result before the next clock cycle comparison. Its response time should be less than the clock period.

Control logic: The digital part of the SAR ADC has 3 operations to perform (Fig. 4 and Fig. 6):

- to control the switches to connect the capacitor plates of the DAC to the appropriate signal to prepare the V_{CNA} signal (DAC output = comparator input) to perform the comparison during one conversion step, with signals S_i,
- to read the comparator result (= decision bit),
- and to store the comparator result (next clock cycle), which is one bit of the digitized signal, B_i.

These operations are performed using:

- The sequencer: It can be described in VHDL, like a Finite State Machine (FSM) and synthesized, or designed based on a circulating-one bank of registers.
- A bank of N registers: to store the conversion bits.

The digital block also includes a clock generator (activating the synchronous comparator, signal Ck or H) and a delayed clock generator (activating the FSM registers and storing of the conversion bits, signal Ck_d or HR).

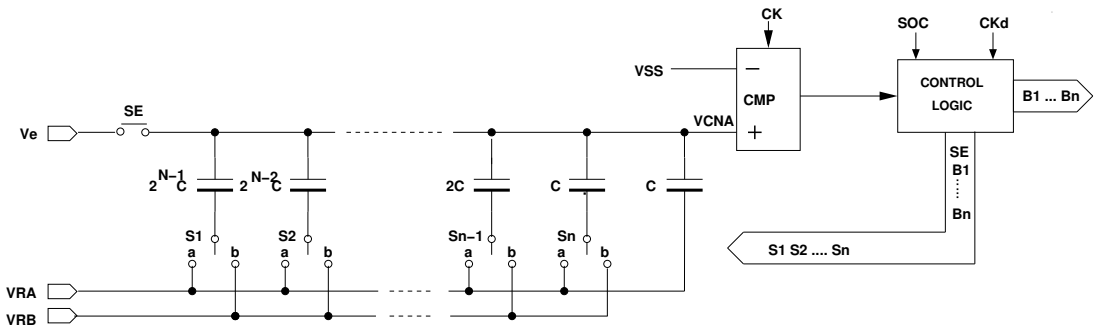

Figure 6: Non differential SAR ADC with implicit sampling using capacitor top plates. Usually $V_{RA} = V_{REF} = V_{DD}$, and $V_{RB} = V_{SS} = 0$. SOC is the Start Of Conversion Signal, an external input signal of the ADC.

2.6 Capacitive DAC

The DAC is the component of the SAR ADC that will have the greatest impact on the ADC performances. Here we give some hints to select the capacitor values and the sizes of the switches.

2.6.1 Capacitor

The capacitor values result from the relation between the ADC accuracy (quantification noise) and the uncertainties due to the thermal noise of the switched capacitors and the mismatch error of the capacitor layout.

Thermal noise consideration

The thermal noise is due to the resistor of the switches, when the switch is on (R_{on}), in the switched capacitor DAC C_s [2]. The noise power can be modelled as a power voltage generator vr^2_{thn} associated to the DAC switched capacitors:

$$vr^2_{thn} = 4K_B T_K R_{on} \tag{8}$$

K_B being the Boltzmann constant T_K the temperature (Kelvin).

The spectrum is white. Moreover the $R_{on}C_s$ establishes a low-pass filtering that makes the spectrum across the sampling capacitor, $v^2_{C,thn}$ coloured.

$$v^2_{C,thn}(\omega) = \frac{4K_B T_K R_{on}}{1 + (\omega R_{on} C_s)^2} \tag{9}$$

The noise power in the band base is given by the integral of the noise power of all the folded bands. This gives a total noise power stored on the sampling capacity C_s when the switch goes off :

$$P_{thn} = K_B T_K / C_s \tag{10}$$

Assuming that the noise budget is such that the thermal noise is less than the quantification noise, gives:

$$K_B T_K / C_s < q^2/12 \tag{11}$$

and,

$$C_s > 12 K_B T_K / q^2 \tag{12}$$

Matching consideration

To take into account the matching error, we consider Fig. 5 with:

$$\frac{V_{CNA}}{V_{REF}} = \frac{C_A}{C_A + C_B} \tag{13}$$

and we assume that the worst case for mismatch corresponds to the half range (i.e. $N = 1000...0$), this configuration corresponds to half of the capacitors

connected to V_{REF} and the other half to ground. If the mismatch error is positive and maximum in a way and negative and maximum on the other way, the mismatch error is maximized. To get the corresponding capacitor area, we recall that:

$$\sigma(\frac{\Delta C}{C}) \approx \frac{1}{\sqrt{2}}\sqrt{\frac{M_a^2}{LW}} \tag{14}$$

where M_a is Pelgrom constant in μm to estimate the mismatch error as function of the device area, and L and W are the sizes of the device area in μm. We will have :

$$\sqrt{LW} \ > \ M_a\frac{3\ .2^N}{\sqrt{2}}. \tag{15}$$

Then, with $C = C_aWL$, C_a being the capacity density, to fulfil the matching specification, we get:

$$C > 9.M_a^2C_a2^{2N-1}. \tag{16}$$

with CPOLY: Ca= $0.3fF/\mu m^2$ Ma=0.01 μm, $C > 0.01pF$ for 8 bits, and $C > 0.15pF$ for 10 bits, and and $C > 2.3pF$ for 12 bits.

Depending on the technology process, the value of the minimum capacitor can be set by matching (Eq. 16) or thermal noise (Eq. 12). It is often mentioned in the literature that the mismatch constraint requires the largest minimal capacitor value. Moreover, an ADC with 12 bits or more require dedicated techniques of capacitor arrays to decrease the whole capacitor area, with more complex control and non binary weighted capacitors.

2.6.2 Switches

The switches connected to low V_{REF}, V_{RB} (usually V_{SS}) are NMOS transistors, (possibly CMOS gate), whereas the switches connected to the high reference voltage V_{RA} (possibly set to V_{DD}) are PMOS transistors (possibly CMOS gate). These transistors have their sources connected to a constant voltage, therefore they make the switched capacitor DAC insensitive to parasitic capacitors present on the bottom plate of the capacitor (which may be as large as C/20), and to the active and passive capacitor present on the transistor drains (which can be fairly large).

The redistribution of charges in the capacitor $C_{(N+1-i)} = 2^{(N-i)}C$ of the DAC, activated by the switch S_i, with its on resistance $R_{i,on}$ operates correctly if the time constant $\tau_i = R_{i,on}C_{(N+1-i)} = R_{i,on}2^{(N-i)}C$ is negligible

with respect to the clock period. Therefore the width W_i of a transistor acting as switch S_i in the DAC is sized to fulfil $\tau_i < T_{ck}$, while its length L_i is minimal. The larger the DAC capacitor value, the smaller the on resistance, and the larger the width.

The switch can be sized depending on the capacitor only, or, to ease the layout, following a binary rule for the width W, or as a multiple of a finger transistor (larger area).

In practice, to take advantage of the available digital standard cell library, it may be useful to replace NMOS/PMOS transistors by inverters (Fig. 7) with appropriate sizes (maybe multi-inverters in parallel) to respect the settling time of the DAC. Typically $V_{REF} = V_{DD}$ to bias all the inverters.

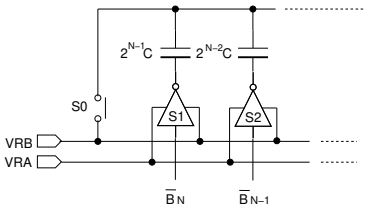

Figure 7: DAC with inverters replacing NMOS/PMOS pairs

2.7 Synchronous comparator

Here we present the comparator of the ADC (Fig. 8). The comparator senses a differential input and generates a logical output according to the polarity of the input difference. According to the ADC architecture, the comparator architecture uses simple input or differential input. We consider comparators based on a bistable (flip-flop) architecture. The synchronous comparator requires a trigger (clock) for the pre-charge phase, therefore requiring a RS flip flop to store the comparator result.

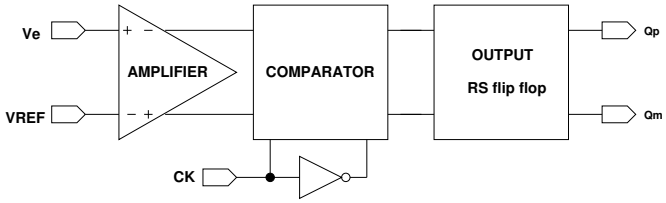

Figure 8: Sub-blocks of the synchronous comparison in Oceane: pre-amplifier, synchronous comparator, RS flip-flop, simple architecture.

2.7.1 Lewis and Gray architecture

Here we discuss the operation mode of the transistors in the Lewis and Gray dynamical comparator (based on a Flip Flop architecture). The main block (Flip Flop, differential architecture, N type) is presented in Fig. 9. The pre-charge phase is active when CK is low and the comparison phase operates when CK is high.

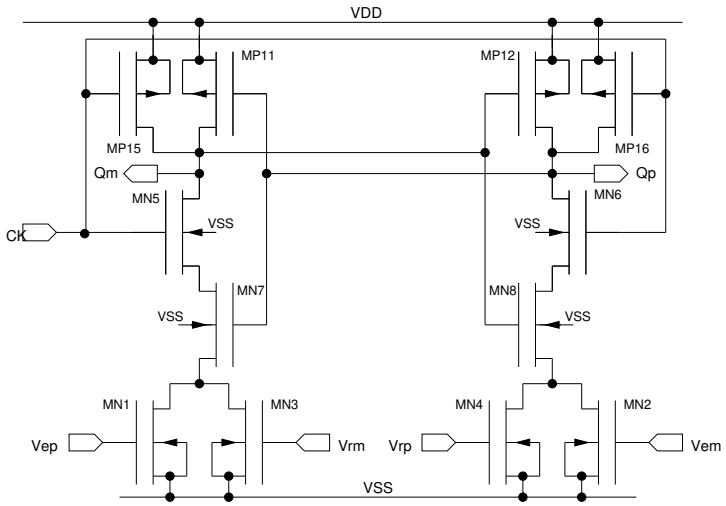

Figure 9: Lewis and Gray comparator in Oceane: main block used in the Lewis and Gray comparator in Fig. 16, differential architecture.

Table 2: Lewis and Gray Comparator, N type, main

transistor names	function	operation mode	L
MN1 MN2, MN3, MN4 Only MN1 and MN2	injection non differential	triode or saturation	Lmin
MN5 and MN6	comparison trigger, on state if CK high	triode (switches)	Lmin
MN7, MP11 and MN8, PM12	2 CMOS inverters bistable	saturation	Lmin
MP15, MP16	pre-charge, CK low	saturation	Lmin

The Lewis and Gray comparator performs a resistive divider (between input -injection- transistors conductance).

2.7.2 Song architecture

Now we discuss the operation mode of the transistors in the Song dynamical comparator (also based on a Flip Flop architecture). The main block (Flip Flop, differential architecture, N type) is presented in Fig. 10. The pre-charge phase is active when CK is low and the comparison phase operates when CK is high.

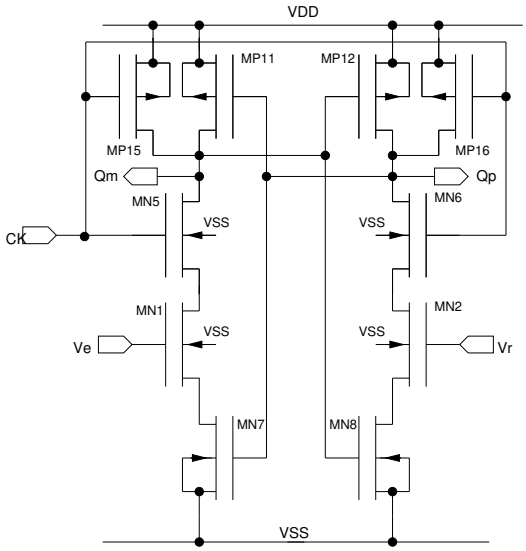

Figure 10: Song comparator (Ntype) in Oceane: main block used in the Song comparator in Fig. 18, differential architecture.

Table 3: Song comparator, N type

transistor names	function	operation mode	L
MN1 and MN2	injection	saturation	Lmin
MN5 and MN6	comparison trigger, on state if CK high		Lmin
MN7, and MN8	2 CMOS	triode, low V_{DS}	Lmin
MP11 and MP12	inverters	bistable	Lmin
MP15, MP16	precharge		Lmin

It is a function similar to Lewis and Gray's one. It often requires larger area, providing less offset voltage.

2.7.3 Dynamical comparator with pre-amplifier and RS output

Synchronous dynamical comparators have good power consumption performances. Yet, architectures based on bistable structures may show large offset voltages and high switching amplitudes. Therefore, in order to decrease the offset voltage, an amplifier can be used at the input of the comparator, so that the effective offset voltage at the comparison input is divided by the amplifier gain. If a dynamical amplifier is used (triggered on clock), then the whole comparison is still dynamical, and the power consumption is low (power consumption only during transitions).

Since the pre-charge phase of the comparator changes the voltage values of the comparator output, an RS flip-flop is used at the comparator output (see Fig. 8) to freeze the comparison result. Moreover, inverters are inserted between the comparator output and the RS flip-flop to decrease meta-stability and dynamical offset.

3 Use case : Sizing a 8bit SAR ADC

In this section we illustrate the sizing process using Oceane FOSS EDA tool by Jacky Porte [3].

3.1 ADC architectures and comparison operation

3.1.1 Non-Differential architecture operation

We first describe the non-differential architecture with implicit sampling using capacitor top plates presented Fig. 6. The conversion follows these operations:

- **Input sampling**

The control signal SE activates the input switch, while the other switches S_i (i=1 to N) set the connections of the capacitor bottom plates to **a** (i.e. all the bits are initially set to **0**, all the capacitor bottom plates are connected to V_{RA}). The positive comparator input V_{CNA} is set to V_e and the following charge Q_1 is stored in the capacitor array:

$$Q_1 = 2^N C(V_e - V_{RA}) \tag{17}$$

- **MSB computation**

In the next clock cycle, the control signal SE disconnects the input signal (the input switch is off), and the switch S_1 sets connection **b**, and the associated $2^{N-1}C$ capacitor bottom plate is connected to V_{RB}, driving $V_{CNA,MSB}$ to the positive comparator input. The redistributed charge is Q_{MSB} and the whole charge conservation in the capacitive array gives:

$$Q_{MSB} \;=\; 2^{N-1}C(V_{CNA,MSB} - V_{RB}) \;+\; 2^{N-1}C(V_{CNA,MSB} - V_{RA}) \qquad (18)$$

and

$$Q_{MSB} = Q_1 \qquad (19)$$

We can derive:

$$V_{CNA,MSB} = V_e - V_{RA} + \frac{V_{RA} + V_{RB}}{2} \qquad (20)$$

and

$$V_{CNA,MSB} = V_e - \frac{V_{REF}}{2}, \quad with \;\; V_{RA} = V_{REF} \quad and \;\; V_{RB} = 0 \qquad (21)$$

If $V_{CNA,MSB} > V_{SS}$, the comparator output is the logical 1 and the MSB value is 1 ($B_{MSB} = 1$), and the switch S_1 keeps the **b** connection (i.e. the bottom plate of the $2^{N-1}C$ capacitor is connected to V_{RB}), otherwise the comparator output is the logical "0", and the MSB is reset to "0" ($B_{MSB} = 0$), and the switch S_1 goes back to the **a** connection (i.e. the bottom plate of the $2^{N-1}C$ capacitor is connected to V_{RA}) .

- **MSB-1 computation**

During the next clock cycle, the (MSB-1) bit is computed, using a similar process. The capacitor bottom plate $2^{N-2}C$ is connected to V_{RB} with switch S_2 set to connection **b**. The charge redistribution and conservation gives:

$$\begin{aligned} Q_{(MSB-1)} \;&=\; B_{MSB}2^{N-1}C(V_{CNA,(MSB-1)} - V_{RB}) \\ &\quad +\overline{B}_{MSB}2^{N-1}C(V_{CNA,(MSB-1)} - V_{RA}) \\ &\quad +2^{N-2}C(V_{CNA,(MSB-1)} - V_{RB}) + 2^{N-2}C(V_{CNA,(MSB-1)} - V_{RA}) \\ &=\; 2^{N}C(Ve - V_{RA}) \end{aligned} \qquad (22)$$

and:

$$V_{CNA,(MSB-1)} = V_e - V_{RA} + \frac{V_{RB}}{2}B_{MSB} + \frac{V_{RA}}{2}\overline{B}_{MSB} + \frac{V_{RB}}{4} + \frac{V_{RA}}{4} \qquad (23)$$

- **LSB computation**

In the following clock cycles, the comparison process is iterated till the LSB ($LSB = MSB - N + 1$), where the input of the comparator, $V_{CNA,LSB}$ is:

$$V_{CNA,LSB} = Ve - V_{RA} + \sum_{i=1}^{N-1} B_{N+1-i}\frac{V_{RB}}{2^i} + \frac{V_{RB}}{2^N} + \sum_{i=1}^{N-1} \overline{B}_{N+1-i}\frac{V_{RA}}{2^i} + \frac{V_{RA}}{2^N}. \quad (24)$$

If $V_{CNA,LSB} > V_{SS}$, $B_{LSB} = 1$, otherwise $B_{LSB} = 0$, and the resulting voltage value V_{ADC}:

$$V_{ADC} = \sum_{i=1}^{N} B_{N+1-i}\frac{V_{RA}}{2^i} + \sum_{i=1}^{N} \overline{B}_{N+1-i}\frac{V_{RB}}{2^i} \quad (25)$$

converges towards the input V_e, i.e. it is the digital representation of the input signal. Usually, V_{RB} is set to zero (V_{SS}) and V_{RA} to V_{REF}. Therefore the switches S_{ia} can be designed with PMOS transistor and switches S_{ib} designed by NMOS ones.

3.1.2 Differential architecture operation

We present now the differential version of the architecture with capacitor top plates input sampling (Fig 11). The differential architecture duplicates the DAC of the non-differential one (Fig.6) on the negative input of the comparator, in a complementary way. The switching of the capacitors belonging to the negative input signal of the comparator (V_{CNAM}) and the switching of the capacitors belonging to the positive input signal of the comparator (V_{CNAP}) are complementary, by inverting V_{RP} and V_{RM} connections. The capacitor C without switch, which has its top plate connected to V_{CNAP}, has its bottom plate directly connected to V_{RP}, while the other capacitor C without switch which has its top plate connected to V_{CNAM}, has its bottom plate directly connected to V_{RM}.

3.1.3 Sampling consideration of the differential architecture

In this differential architecture (Fig 11), the differential input signal which has to be converted is sampled by the switches SE (on) during the first cycle on the top plates of the DAC capacitors. When the MSB Preset strategy is used, the MSB is also set to 1. During the first comparison, S_{1a} is "b-connected" (with MSB set to one) and the charge is redistributed between the

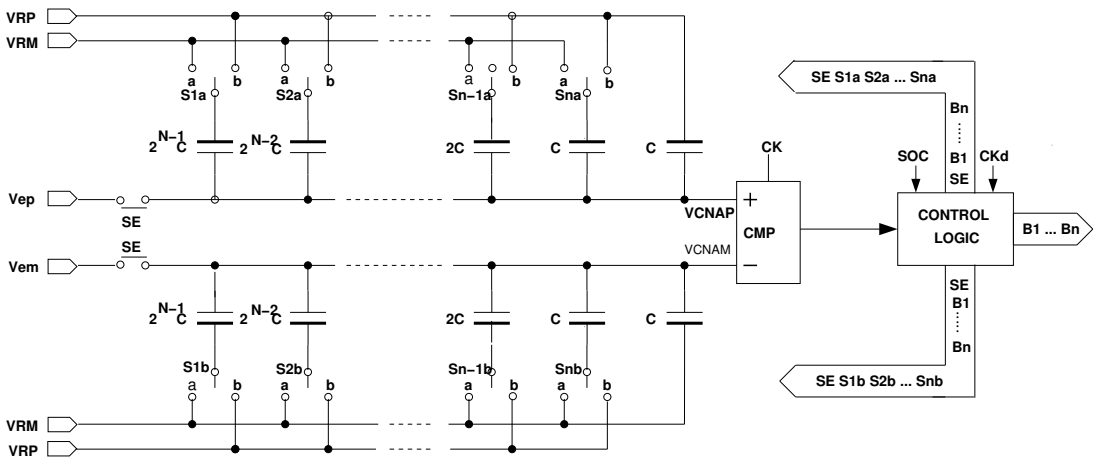

Figure 11: differential SAR ADC with top plate implicit sampling

DAC capacitors to control V_{CNAP} and V_{CNAM} the 2 inputs of the comparator (Fig. 12).

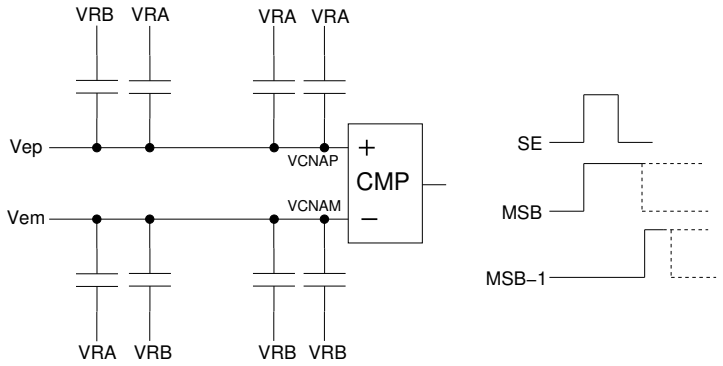

Figure 12: First comparison setting of the differential architecture with top plate implicit sampling and MSB Preset strategy

3.2 Digital Control

3.2.1 Sequencer

Fig. 13 illustrates one possible realisation of the sequencer, as a Finite State Machine (FSM).

Each state is a conversion step in the binary search algorithm. The output sets the control of the DAC switches to set the appropriate input of the

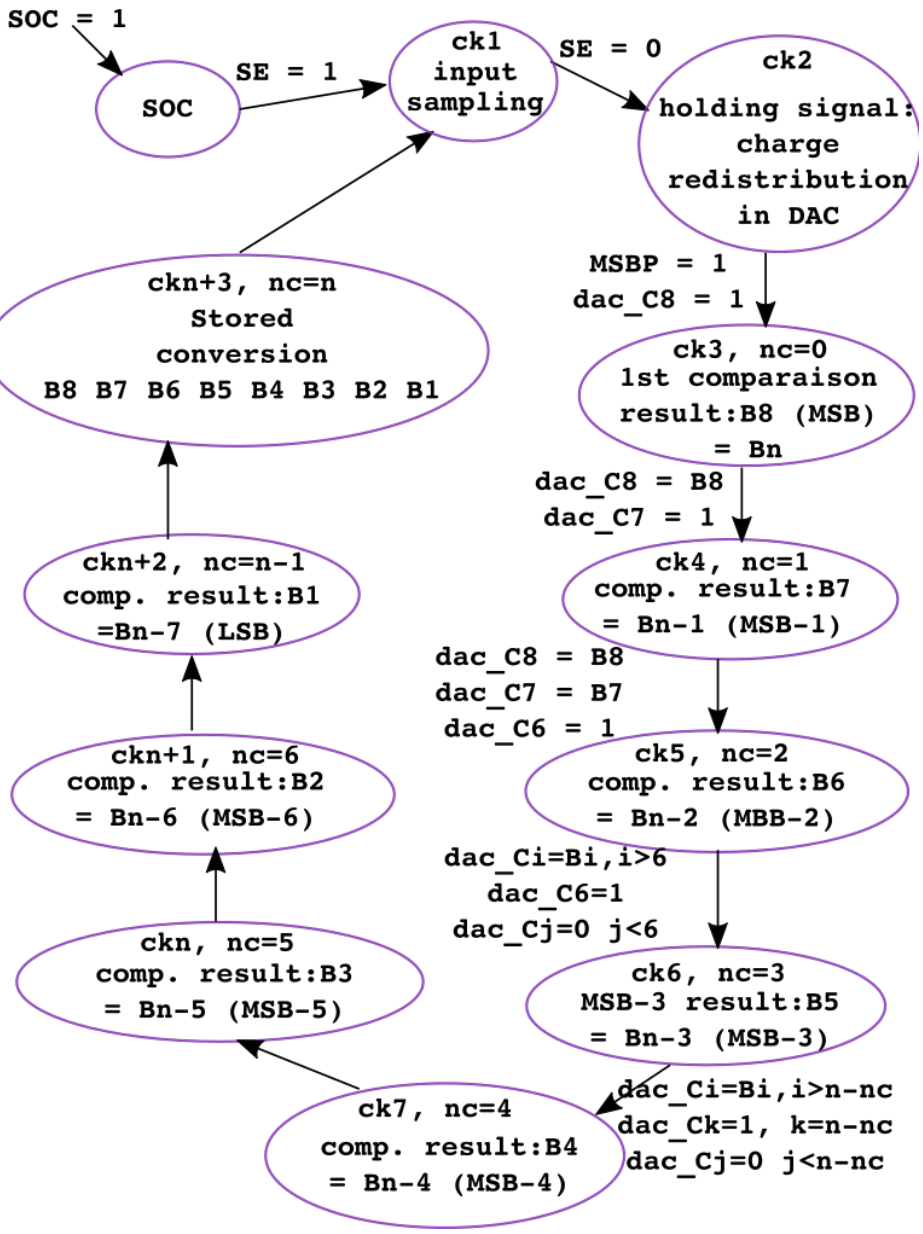

Figure 13: Finite State Machine of the differential SAR ADC with implicit sampling with $N = 8$

converter for the next conversion step. The initial states are used to sample and hold the input signal, when the Sample Enable (SE) signal is raised. The conversion is activated by the Start Of Conversion (SOC) signal. At the end of the conversion cycle, a signal End Of Conversion (EOC) is generated to

validate the ($N = 8$) bits.

Oceane uses a structural direct approach to design the digital control block presented:

- Fig. 14 in a non-differential ADC architecture, with top plate implicit sampling, and
- Fig. 15 in a differential ADC architecture, with top plate implicit sampling and MSB Preset strategy.

In these topologies (Fig. 14 and Fig. 15), the ($i + 1$) register of the sequencer activates the registration of the (i) bit (B_i) of the digital conversion. 2 inverters are used to delay the clock from the synchronous comparator ($Ck = H$) to the sequencer ($Ck_d = HR$).

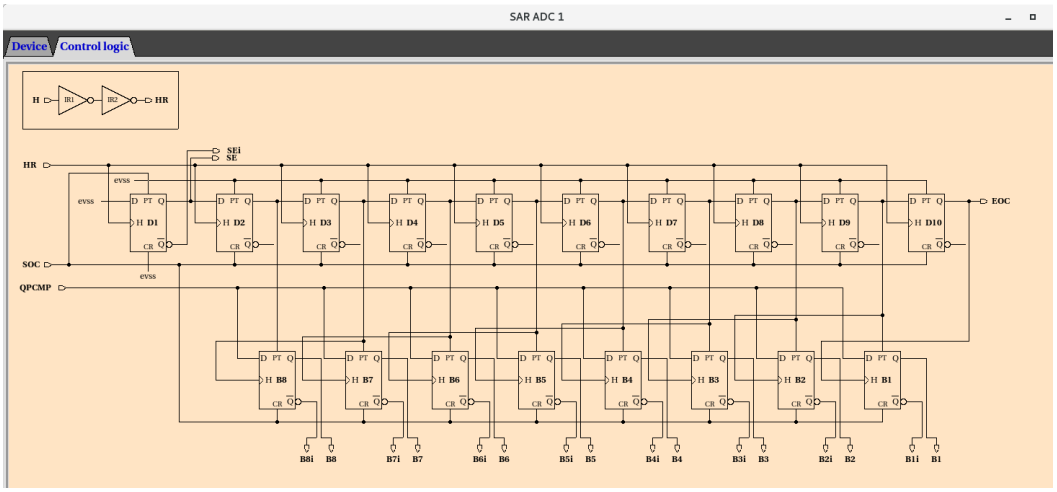

Figure 14: Oceane digital control block, non-differential ADC architecture, with capacitor top plates implicit sampling

In the differential case (Fig. 15), the MSB preset strategy is used, therefore the MSBP signal is generated.

3.2.2 Storing the N conversion bits

N registers (Flip-Flops) are necessary to store the conversion result, B_8 to B_1 (Fig. 14 and Fig. 15). The conversion requires (N+2) clock cycles to get the whole 8 bit word in the non-differential architecture (D_1 to D_{10} in Fig. 14) and (N+3) clock cycles in the differential one (D_1 to D_{11} in Fig. 15).

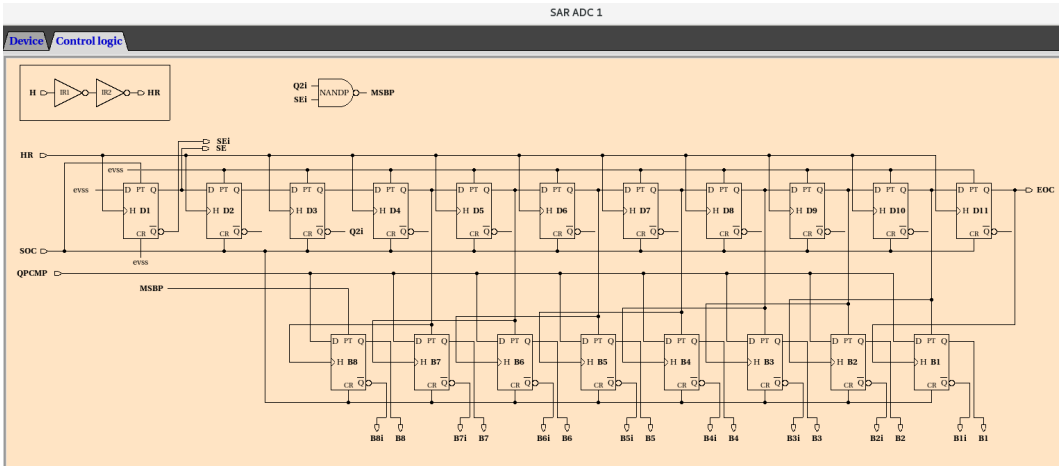

Figure 15: Oceane digital control block, differential ADC architecture, with capacitor top plates implicit sampling and MSB Preset strategy

3.3 DAC capacitor and switches

3.3.1 Capacitors

We refer to paragraph 2.6.1 and to the technology Process Design kit to size the capacitors. Here we choose $C_{min} = 0.5pF$ as an example. For $N = 8$ bits, we need, a total capacity of $CT = 128pF$, in the non differential case, and $CT = 256pF$, in the differential case.

The binary weighted capacitors are as follows (F):

```
C0 5.000000e-13
C1 5.000000e-13
C2 1.000000e-12
C3 2.000000e-12
C4 4.000000e-12
C5 8.000000e-12
C6 1.600000e-11
C7 3.200000e-11
C8 6.400000e-11
```

3.3.2 Switches

We refer to paragraph 2.6.2 to select the appropriate switches. Here we use NMOS transistors to set the connexion **b** (capacitor bottom plates to V_{SS}) and PMOS transistors to set the connexion **a** (capacitor bottom plates to V_{DD}). We use a modular sizing approach: the smallest switch (activating the smallest capacitor, C_1) is sized, and the other switches are sized as multiple, possibly over sized, but with easier layout generation.

3.4 Comparator

3.4.1 Synchronous Architectures

In the non-differential architecture, we can use a synchronous comparator (Ck clocked) with dynamic preamp (P type dynamic pre-amplifier and P type Lewis and Gray P type flip-flop loaded with inverters acting as buffers) shown in Fig. 16.

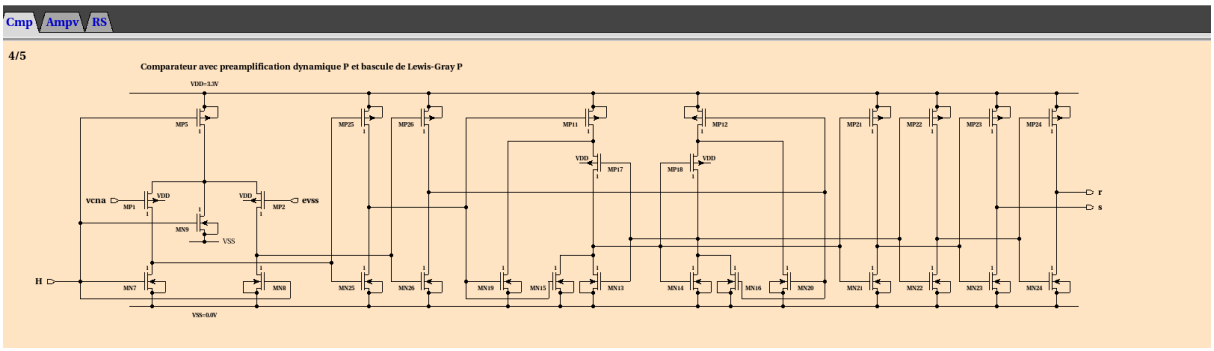

Figure 16: Oceane comparator: main block, P type dynamic pre-amplifier and Lewis and Gray P type Flip Flop, loaded with inverters acting as buffers used for the non-differential ADC

The output is stabilized with a bistable RS output presented in Fig. 17, to keep the comparator output constant during the precharge phase of the synchronous comparator.

In the differential architecture we can also use the synchronous comparator (Ck clocked) with dynamic preamp (P type dynamic pre-amplifier and N type Song type flip-flop loaded with inverters) shown in Fig. 18, with its Flop Flop (Fig. 19) at the output.

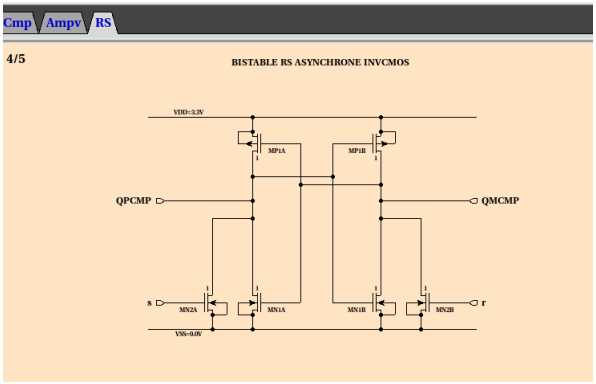

Figure 17: Oceane comparator output: RS FlipFlop based on inverters, for comparator in Fig. 16

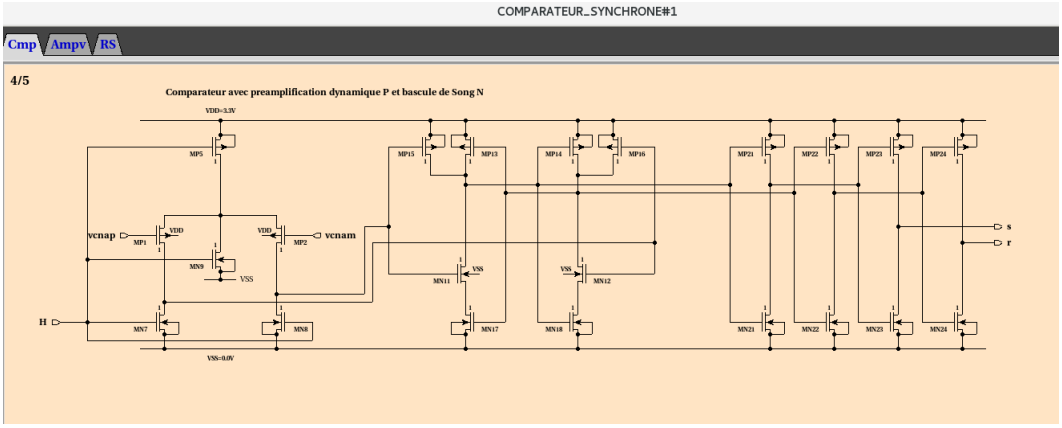

Figure 18: Oceane comparator: main block, P type dynamic pre-amplifier and N type Song type Flip Flop used for the differential ADC

3.4.2 Sizing

The comparator relevant performances for the SAR ADC are the response time (less than one clock cycle) and the offset (less than one LSB).

The sizing trade-off are, as usual between speed and accuracy:

- Increasing the transistor's length L
  - Improves matching (decreases offset of the comparator)
  - Improves power consumption
  - Increases the response time

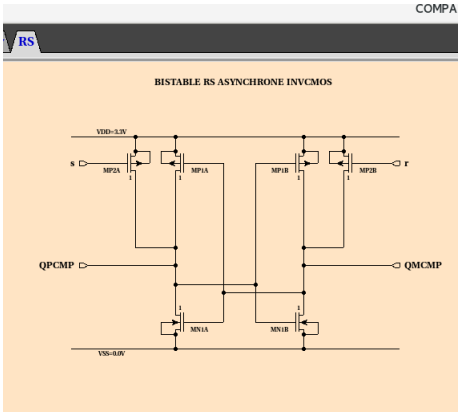

Figure 19: Oceane comparator output: RS FlipFlop based on inverters, for the comparator in Fig. 18

- Decreasing the transistor's length L
  - Improves the response time
  - A standard default value : L_{min} to optimize the response time
  - Increases offset

Table 4: Song comparator, N type with P type pre-amplifier (Fig. 18)

transistor names	function	operation mode	L
MP1 and MP2	injection	saturation strong inversion	offset impact
MP5	comparison trigger, on state if CK high	triode strong inversion	Lmin
MN6, MN7 and MN9	precharge	saturation low inversion	Lmin Lmin
MN11 and MN12	injection	saturation strong inversion	Lmin
MN17, and MN18 MP13 and MP14	2 CMOS inverters	strong inv. bistable	Lmin or L
MP15, MP16	precharge	saturation low inversion	Lmin or L

will provide a response time around 200 pS.

4 Scalability

Here we study the relevant parameters to migrate the differential ADC in another technology node or according to another set of specifications in the same technology node.

Note that the design of the passive components, here the capacitors for the DAC, are specific to a technology node.

4.1 Differential architecture

4.1.1 ADC level parameters

The ADC differential architecture is set as follows (Table. 5):

Table 5: Differential ADC architecture choices

Input sampling	capacitor top plate, implicit S/H
Differential	DAC: 2.(N+1) capacitors, total $2^{N+1}C$
Reference voltage	VDD, no additional voltage
Input switch	2 PMOS (capacitor top plates)
Switches for DAC	$2N$ NMOS and $2N$ PMOS transistors (capacitor bottom plates) or more, depending on the layout aware sizing constraints.
Comparator	Synchronous (pre-amplifier and Flip-Flop) with RS output
Control logic	Sequencer as register bank (circulating one) Conversion bit i storing activated by the $i+1$ register

This architecture requires the following parameters (Table. 6):

4.1.2 Control logic parameters

The digital block contains the sequencer, the decoder, the signals controlling the whole conversion sequence, the clock signals and the conversion result (N bits) parameters (Table 7).

4.1.3 DAC level parameters

The DAC parameters concern the capacitors, where C_{min} is derived from technological process and the ADC accuracy, as well as switches to control the switching of the capacitors (Table 8).

Table 6: Differential ADC specification parameters

Parameter	Note	350 node	350 node	180 node	130 node
V_{DD}	power supply (V)	3.3	3.3	1.8	1.8
V_{SS}	ground supply (V)	0	0	0	0
V_{REF}	reference voltage (V) to handle converter input range and distortion	3.3	3.3	1.8	1.8
V_{EMC}	input common mode (V)	1.65	1.65	0.9	0.9
V_{emax}	input value (V) used for simulation	2.64	2.64	1.44	1.44
N	number of bits	8	8	8	8
F	clock Frequency (Hz)	10^6	10^7	10^6	10^6
C	minimum value (F)	0.5^{-12}	0.5^{-12}	0.1^{-12}	0.1^{-12}
Temperature	nominal (C)	27	27	27	27

Table 7: Sequencer, decoder and registers, differential ADC architecture

Function	Note	Cells
Sequencer	FSM or circulating one	$N + 2 = 10$ registers
Control signals	SOC and EOC and MSB	
Decoder	Switch control logic depending on comparator output and state (iteration) number	
Conversion bits	ADC result	$N = 8$ registers
Clock	comparator and control block	Ck and delayed Ck

4.1.4 Comparator parameters

The selected architecture (Fig.18) is a synchronous comparator with dynamic pre-amplifier (P type dynamic pre-amplifier with Ntype Song Flip-Flop) requires the parameters presented in Table 9.

Table 8: DAC parameters used in differential ADC architecture

Capacitor	Note	Value
$2(N+1)$ capa	binary weighted	C_{min} from matching performance
Switches	NMOS	$2(N+1)$ switches, modular sizing
Switches	PMOS	$2(N+1)$ switches, modular sizing

Table 9: Comparator parameters used in differential ADC architecture

Parameter	Note	350 node	180 node	130 node
V_{DD}	power supply (V)	3.3	1.8	1.8
V_{SS}	ground supply (V)	0	0	0
V_{RP}	reference voltage (V)	1.65	0.9	0.9
E_d	static offset voltage (V) standard deviation not directly related to $q = V_{REF}/2^N$	$10mV$	$10mV$	$10mV$
F	clock Frequency (Hz) 10 times the ADC clock frequency	10^7	10^7	10^7
C load	(F)	0.01^{-12}	0.01^{-12}	0.01^{-12}

4.1.5 Simulation results

Fig. 20 presents the comparator input and output signals for the 8-bit, differential SAR ADC architecture operating at Ck = 1 MHz.

Fig. 21 presents the comparator input and output signals for the 8-bit, differential SAR ADC architecture operating at Ck = 10 MHz.

Fig. 22 presents the MSB signals for the 8 bit, differential SAR ADC architecture operating at Ck = 10 MHz.

5 Conclusion

This document summarizes the ongoing work performed by Jacky Porte at Sorbonne Université-LIP6 to integrate SAR ADC sizing into Oceane, a FOSS EDA tool. Today it is only possible to perform the sizing in a 350nm technology node, since this technology has a rue BSIM compact model.

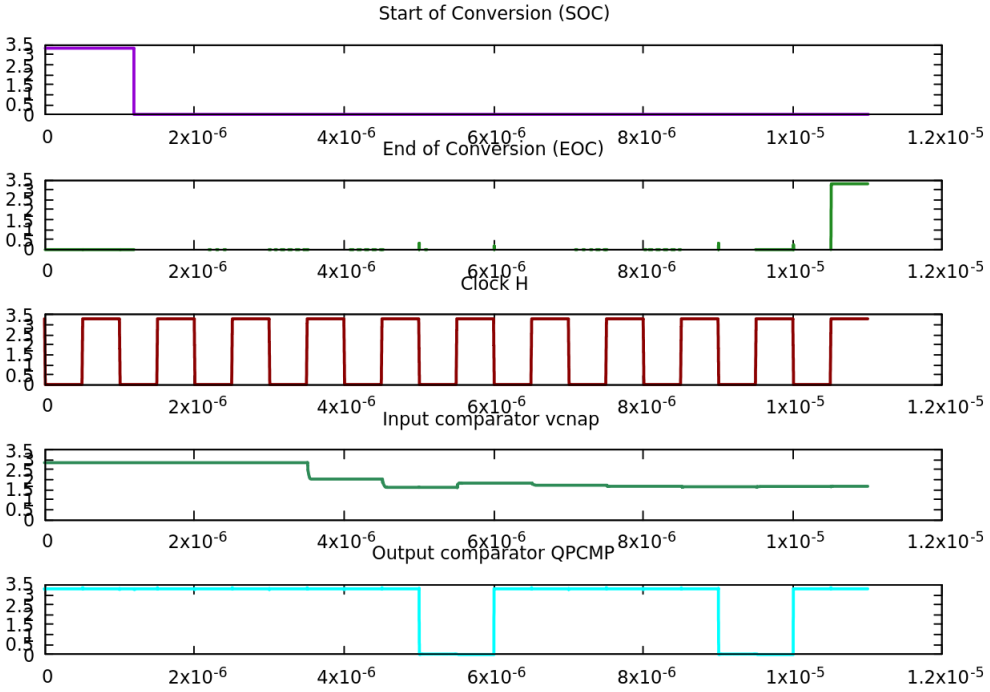

Figure 20: Oceane differential SAR ADC (Fig. 11), capacitor top plates implicit sampling, 8 bit, $ve_{diff} = 2.409V$, 1MHz, simulation results.

Sizing examples were presented, to illustrate the performance of existing architectures which allow to reach 8 to 10 bits, at CK=10 MHz maximum for one bit (whole conversion CK/N).

Ongoing work addresses bootstrap switches (for explicit S/H) and other technology nodes.

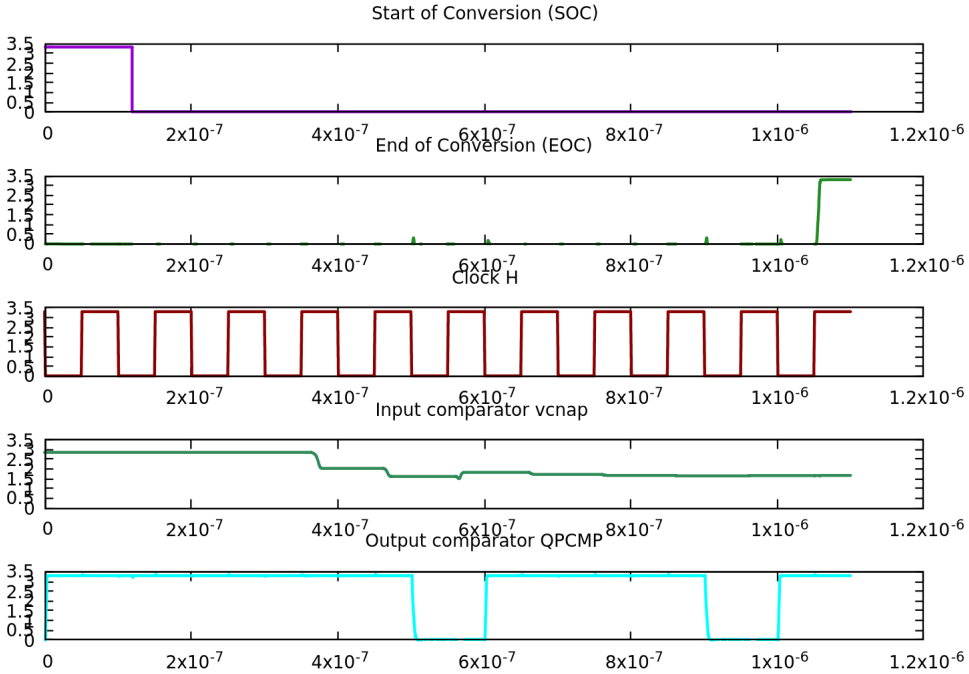

Figure 21: Oceane differential SAR ADC (Fig. 11), capacitor top plates implicit sampling, 8 bit, $ve_{diff} = 2.409V$, 10MHz, simulation results.

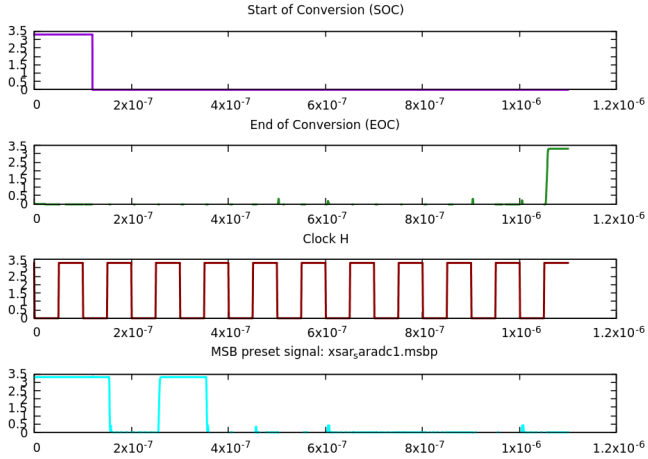

Figure 22: Oceane differential SAR ADC (Fig. 11), capacitor top plates implicit sampling, 8 bit, $ve_{diff} = 2.409V$, 10MHz, simulation results, MSBP.

6 List of Acronyms

ADC	Analogue-to-digital Converter
DAC	Digital-to-Analogue Converter
CMOS	Complementary Metal Oxide Semi-Conductor
DC	Direct Current (DC analysis or operating point)
EOC	End Of Conversion, to validate the result
SE	Sample Enable signal to activate the input sampling
FSM	Finite State Machine(sequencer of the SAR ADC)
LSB	Least Significant Bit
MSB	Most Significant Bit
MSBP	Most Significant Bit Preset
SAR ADC	Successive Approximation Register Analog-to-digital Converter
SOC	Start Of Conversion, signal to activate the conversion cycle.
V_{DD}	Voltage power supply
V_{emax}	Input range to set the comparator input, it should be less than the power supply voltage
V_{REF}	Reference Voltage to perform the conversion steps, it can be equal to the power supply voltage

References

[1] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. MacGraw-Hill, 2001.

[2] Franco Maloberti. *Data Converters*. Springer, first edition, 2007.

[3] Jacky Porte. *Oceane - ADC design*. LIP6, 2022.

Appendix

In this appendix we provide some other considerations and insights for the interested reader.

Other Sizing Consideration

The capacitor values result from the relation between the ADC accuracy (quantification noise) and the uncertainties due to the thermal noise of the switched capacitors and the mismatch error of the capacitor layout.

Thermal noise consideration

The following model (Fig. 23) refers to the capacitive divider (Fig. 5) of the explicit sampling architecture (Fig. 4) presented in section (2.4).

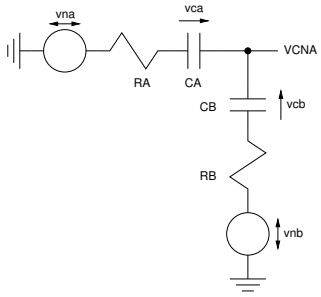

Figure 23: Model for noise consideration of the ADC in the explicit sampling type architecture (Fig. 4)

The thermal noise is due to the resistor of the switches, when the switch is on (R_{on}), in the switched capacitor DAC. The noise power can be modelled as a power voltage generator vr^2_{thn} associated to the DAC switched capacitors:

$$vr^2_{thn} \;=\; 4K_B T_K R_{on} \tag{26}$$

K_B being the Boltzmann constant T_K the temperature (Kelvin). Two types of noise (uncorrelated) exist in such switched capacitor circuits: a wide band "direct" noise, which can be computed using continuous time techniques, and a noise resulting from the quantification. On the DAC output, i.e. the comparator input, the "direct" noise should only be taken into account. Assuming that C_x is neglected, considering sampled voltages by C_A and C_B controlled by B_i and $\overline{B_i}$, at the end of the switching step, we use the low pass model of Fig. 23 and consider the low pass transfer functions:

$$v_{ca} \;=\; \frac{C_B}{C_A+C_B}\;\frac{vna \;+\; vnb}{(R_A+R_B)\frac{C_AC_B}{C_A+C_B}p+1} \tag{27}$$

and

$$v_{cb} \;=\; \frac{C_A}{C_A+C_B}\;\frac{vna \;+\; vnb}{(R_A+R_B)\frac{C_AC_B}{C_A+C_B}p+1} \tag{28}$$

with:

$$vn_{ca}^2 \;=\; 4K_BT_K(R_A+R_B)\int_0^\infty |H(j\omega)|^2 df \tag{29}$$

and

$$\int_0^\infty |H(j\omega)|^2 df \;=\; \frac{C_B^2}{(C_A+C_B)^2}\frac{\omega_c}{4} \tag{30}$$

we get

$$vn_{ca}^2 \;=\; K_BT_K\frac{C_B}{C_A(C_A+C_B)} \tag{31}$$

and

$$vn_{cb}^2 \;=\; K_BT_K\frac{C_A}{C_B(C_A+C_B)} \tag{32}$$

The comparator input referred noise is:

$$v_{thn}^2 \;=\; \frac{K_BT_K}{C_A+C_B}(\frac{C_A}{C_B}+\frac{C_B}{C_A}) \;=\; \frac{K_BT_K}{2^NC}(\frac{C_A}{C_B}+\frac{C_B}{C_A}). \tag{33}$$

This noise power depends on the input signal, and changes at each step of the conversion process. It is minimum for:

$$v_{thn}^2 \;=\; \frac{K_BT_K}{2^{N-1}C} \tag{34}$$

when MSB is computed ($C_A = C_B$), and maximum for:

$$v_{thn}^2 \;=\; \frac{K_BT_K}{2^NC}(\frac{C_A}{2^NC-C_A}+\frac{2^NC-C_A}{C_A}) \;\approx\; \frac{K_BT_K}{C} \tag{35}$$

when LSB is computed ($C_A = C$). As it should be less than the intrinsic quantification noise of the ADC, which is:

$$v_{qn}^2 \;=\; \frac{q^2}{12} \;\; with \;\; q \;=\; \frac{V_{REF}}{2^N} \tag{36}$$

the minimum value of C is computed as follows:

$$\frac{K_BT_K}{C} \;<\; \frac{q^2}{12} \; or \; C \;>\; 12\frac{K_BT_K}{q^2}. \tag{37}$$

As shown in Table 10, due to the required area of the capacitive DAC, it is difficult to design an ADC with explicit sampling, for N greater than 10, also considering the low voltage power supply.

Please note that we considered the explicit sample and hold architecture to derive these equations. In the literature, you may often see the "$\frac{K_B T_K}{C_s}$" relation used, where C_s is computed as the sampling capacitor.

N =	4	6	8	10	12	14	16
V_{REF} = 0.5 V	C=50aF	C=0.81fF	C=13.03fF	C=208.6fF	C=3.34pF	C=53.4pF	C=854.3pF
V_{REF} = 1 V	C=12.7aF	C=0.2fF	C=3.25fF	C=52.14fF	C=0.83pF	C=13.34pF	C=213.5pF
V_{REF} = 2 V	C=3.1aF	C=0.05fF	C=0.81fF	C=13.03fF	C=0.20pF	C=3.33pF	C=53.4pF
V_{REF} = 4 V	C=0.8aF	C=0.012fF	C=0.20fF	C=3.26fF	C=0.05pF	C=0.83pF	C=13.34pF

Table 10: Thermal noise consideration: Minimum values of C as function of N and V_{REF} at $T = 27^oC$

Matching consideration
To take into account the matching error, we consider Fig. 5 with:

$$\frac{V_{CNA}}{V_{REF}} = \frac{C_A}{C_A + C_B} \tag{38}$$

and we assume that the worst case for mismatch corresponds to the half range (i.e. $N = 1000...0$), this configuration corresponds to half of the capacitors connected to V_{REF} and the other half to ground. If the mismatch error is positive and maximum in a way and negative and maximum on the other way, the mismatch error is maximized. We define:

$$C = \hat{C}(1 \pm 3\sigma(\frac{dC}{C})) \tag{39}$$

with $\sigma(\frac{dC}{C})$ being the standard deviation on local mismatch resulting from the capacitor C mismatch, and we get:

$$\frac{V_{CNA}}{V_{REF}}|_{MSB} = \frac{2^{N-1}\hat{C}(1+3\sigma(\frac{dC}{C}))}{2^{N-1}\hat{C}(1+3\sigma(\frac{dC}{C})) + 2^{N-1}\hat{C}(1-3\sigma(\frac{dC}{C}))} = \frac{1}{2}(1+3\sigma(\frac{dC}{C})) \tag{40}$$

The maximal error at middle point (i.e. half range) should verify:

$$\frac{1+3\sigma(\frac{dC}{C})}{2} - \frac{1}{2} < \frac{1}{2^{N+1}} \quad or \quad 3\sigma(\frac{dC}{C}) < \frac{1}{2^N} \tag{41}$$

to be less than $q/2$. To get the corresponding capacitor area, we recall that:

$$\sigma(\frac{\Delta C}{C}) \approx \frac{1}{\sqrt{2}}\sqrt{\frac{M_a^2}{LW}} \tag{42}$$

where M_a is Pelgrom constant in μm to estimate the mismatch error as function of the device area, and L and W are the sizes of the device area. We will have :

$$\sqrt{LW} \ > \ M_a\frac{3\ .2^N}{\sqrt{2}}. \tag{43}$$

Then, with $C = C_aWL$, C_a being the capacity density, to fulfil the matching specification, we get:

$$C > 9.M_a^2C_a2^{2N-1}. \tag{44}$$

with CPOLY: Ca= $0.3fF/\mu m^2$ Ma=0.01 μm, $C > 0.01pF$ for 8 bits, and $C > 0.15pF$ for 10 bits, and and $C > 2.3pF$ for 12 bits.

Depending on the technology process, the value of the minimum capacitor can be set by matching (Eq. 16) or noise (Table 10). It is often mentioned in the literature that the mismatch constraint requires the bigger minimal capacitor value. Moreover, an ADC with 12 bits or more require dedicated techniques of capacitor arrays to decrease the area, with more complex control and non binary weighted capacitors.

Non Differential architecture scalability

Here we give some hints to migrate the non-differential ADC in another technology, or with a different set of performances within the same node.

Note that the design of the passive components, here the capacitors for the DAC, are specific to a technology node.

ADC level parameters

The non-differential ADC architecture is set as follows (Table. 11):

This architecture requires the following parameters (Table 12):

Control logic parameters

The digital block contains the sequencer, the decoder, the signals controlling the whole conversion sequence, the clock signals and the conversion result (N bits) parameters (Table 13).

Table 11: ADC architecture choices, non-differential architecture

Input sampling	capacitor top plate, implicit S/H
Non differential DAC	DAC: $(N+1)$ capacitors, total capacitor value $= 2^N C$ Capacitor type (layer, value) depend a lot on the technology node.
Reference voltage	VDD, no additional voltage
Input switch	one PMOS (capacitor top plates)
Switches for DAC	N NMOS and N PMOS transistors (capacitor bottom plates) may be more, depending on the layout aware sizing constraints.
Comparator	Synchronous (pre-amplifier and Flip-Flop) with RS output
Control logic	Sequencer as register bank (circulating one) control of the DAC switches Conversion bit i storing activated by the $i+1$ register

Table 12: ADC specification parameters, non-differential architecture

Parameter	Note	350 node	350 node	180 node	130 node
V_{DD}	power supply (V)	3.3	3.3	1.8	
V_{SS}	ground supply (V)	0	0	0	0
V_{REF}	reference voltage (V) to handle converter input range and distortion	3.3	3.3	1.8	
V_{EMC}	input common mode (V) VDD/2 is required	1.65	1.65		
V_{emax}	input value (V) used for simulation	2.64			
N	number of bits	8	10	8	
F	clock Frequency (Hz)	10^6	10^6	10^6	
C	minimum value (F) example	0.5^{-12}	0.5^{-12}		

Table 13: Sequencer, decoder and registers, non differential ADC

Function	Note	Cells
Sequencer	FSM or circulating one	$N + 2 = 10$ registers
Control signals	SOC and EOC	
Decoder	Switch control logic depending on comparator output and state (iteration) number	
Conversion bits	ADC result	$N = 8$ registers
Clock	comparator and control block	Ck and delayed Ck

DAC level parameters

The DAC parameters concern the capacitors, where C_{min} is derived from technological process and the ADC accuracy, as well as switches to control the switching of the capacitors (Table 14).

Table 14: DAC parameters used in the non-differential ADC architecture

Capacitor	Note	Value
$N + 1$ capa	binary weighted	C_{min} from matching performance
Switches	NMOS	$N + 1$ switches, modular sizing
Switches	PMOS	$N + 1$ switches, modular sizing

Comparator parameters

The selected architecture (Fig.16) is a synchronous comparator with dynamic pre-amplifier (P type dynamic pre-amplifier with Lewis and Gray Flip-Flop) which requires the following parameters (Table 15):

Simulation results

Fig. 24 presents the comparator input and output signals for the 8-bit, non differential SAR ADC architecture operating at Ck = 1MHz.

Fig. 25 presents the comparator input and output signals for the 10-bit, non differential SAR ADC architecture operating at Ck = 1MHz.

Table 15: Comparator parameters in the non differential ADC case

Parameter	Note	350 node	180 node	130 node
V_{DD}	power supply (V)	3.3	1.8	
V_{SS}	ground supply (V)	0	0	0
V_{RP}	reference voltage (V)	0	0	0
E_d	static offset voltage (V) standard deviation (example) not directly related to $q = V_{REF}/2^N$	$10mV$		
N	number of bits	8		
F	clock Frequency (Hz) 10 times the ADC clock frequency	10^7		
C load	(F)	0.01^{-12}		

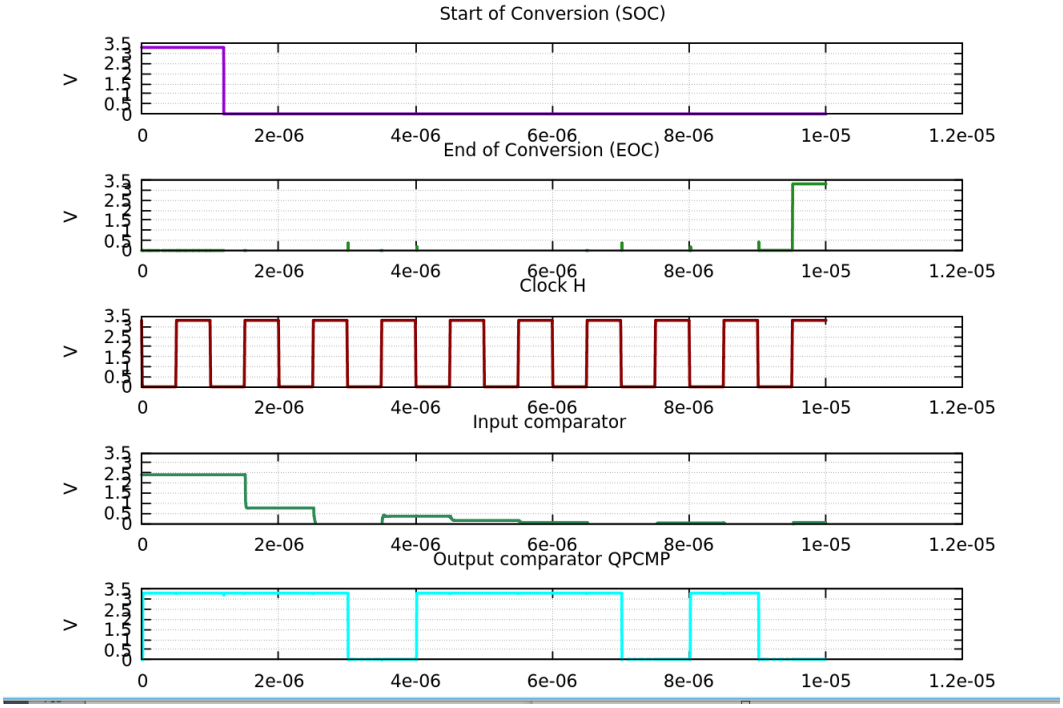

Figure 24: Oceane non-differential SAR ADC (Fig. 6), capacitor top plates implicit sampling, 8 bit, ve = 2.409 V, CK = 1MHz, simulation result.

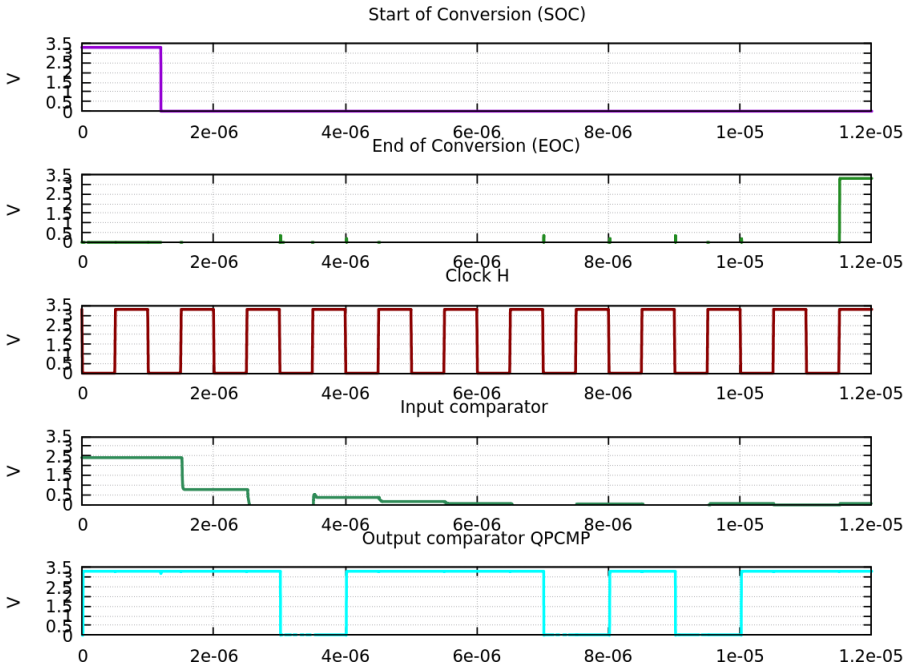

Figure 25: Oceane non-differential SAR ADC (Fig. 6), capacitor top plates implicit sampling, 10 bit, ve = 2.409 V, Ck = 1MHz, simulation result.